

FIG. 1

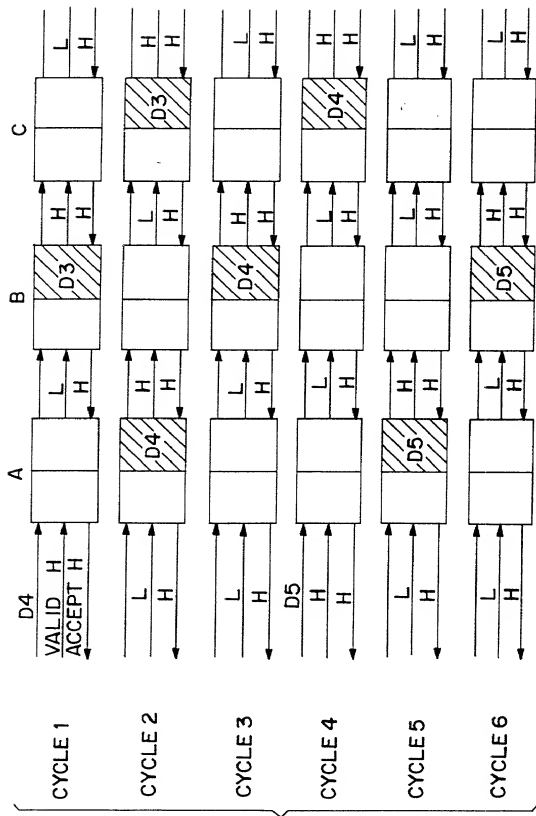


FIG. 2(A)

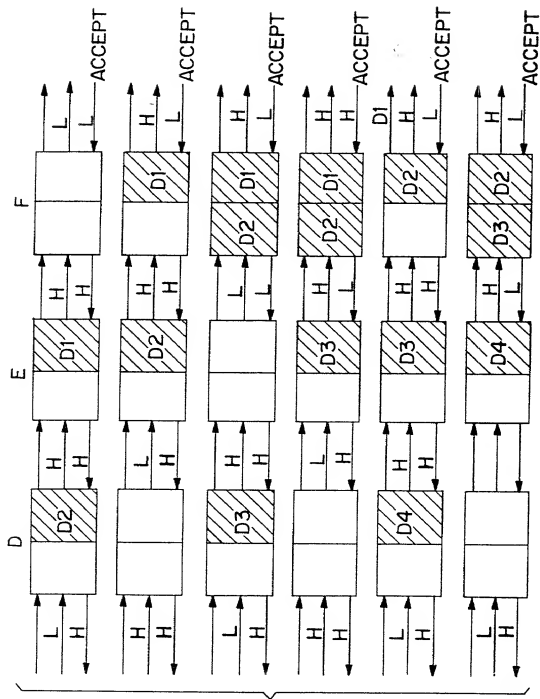
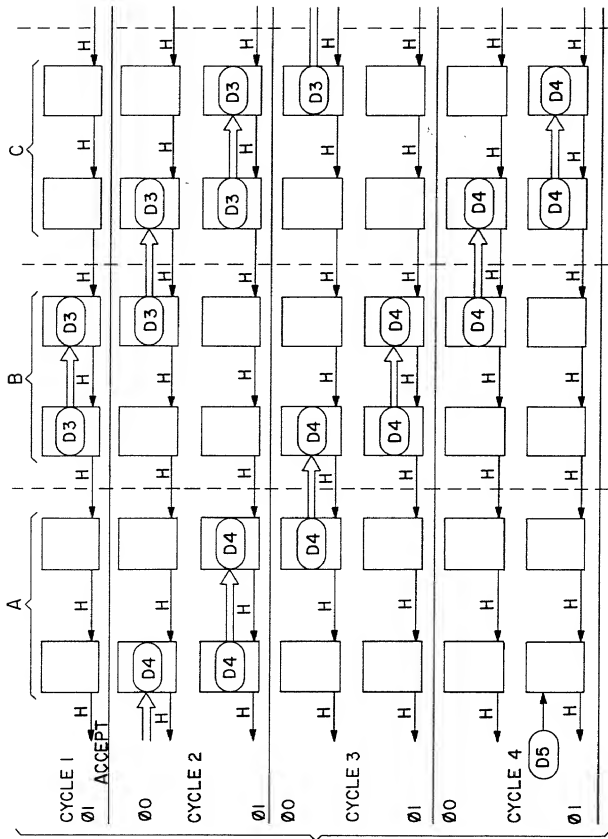
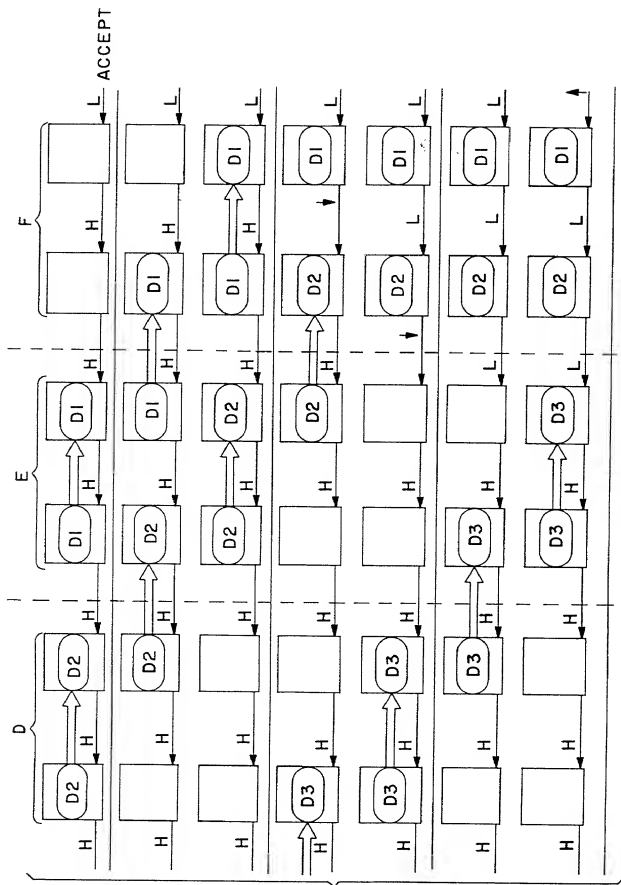


FIG. 2(B)





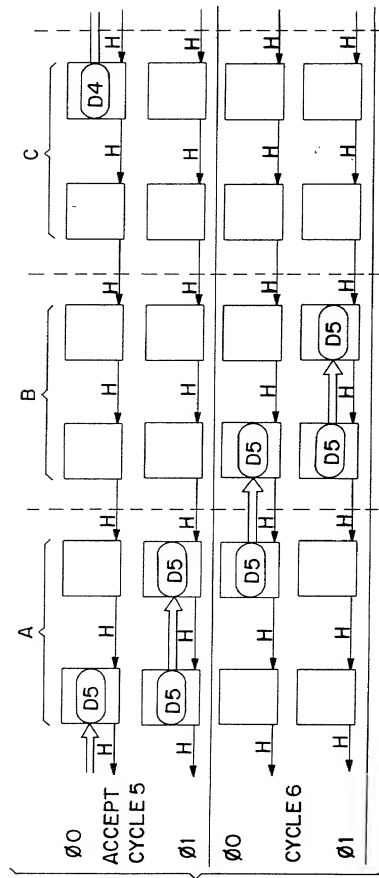


FIG. 3B-1

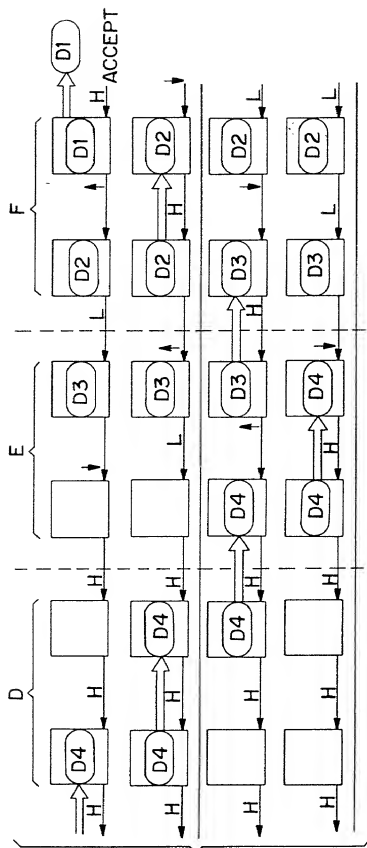


FIG. 3B-2

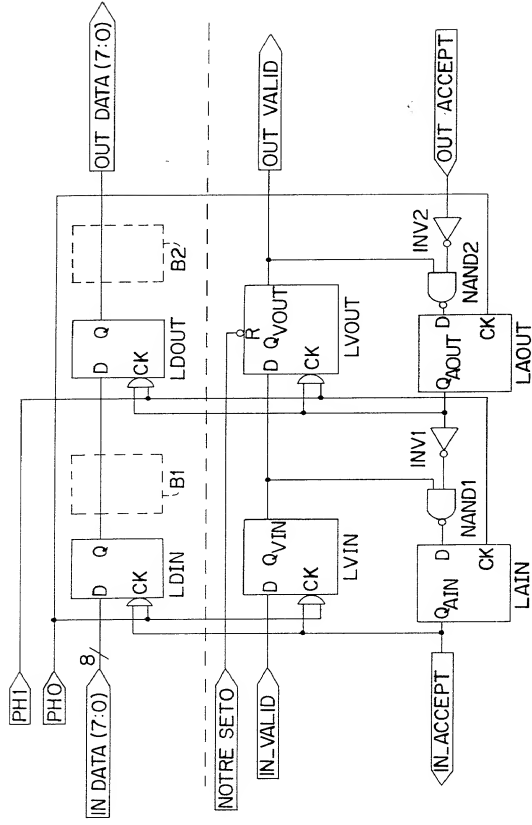


FIG. 4

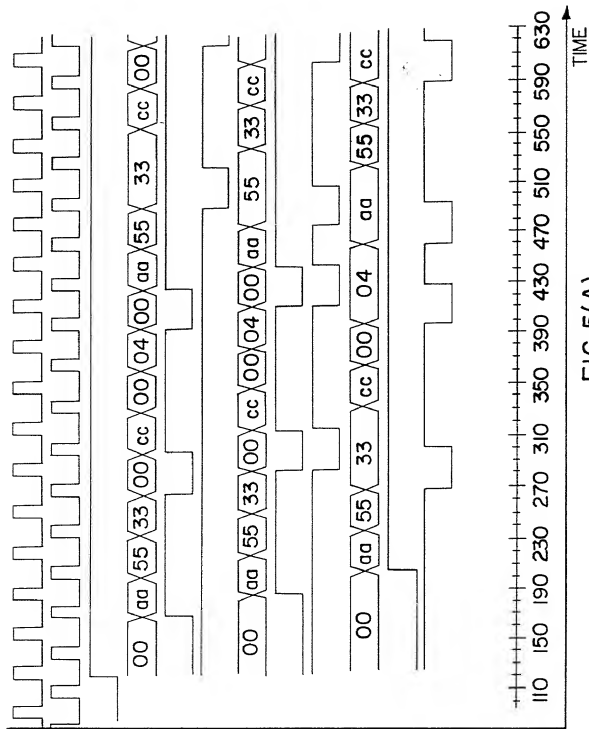


FIG. 5(A)

00726696-015001

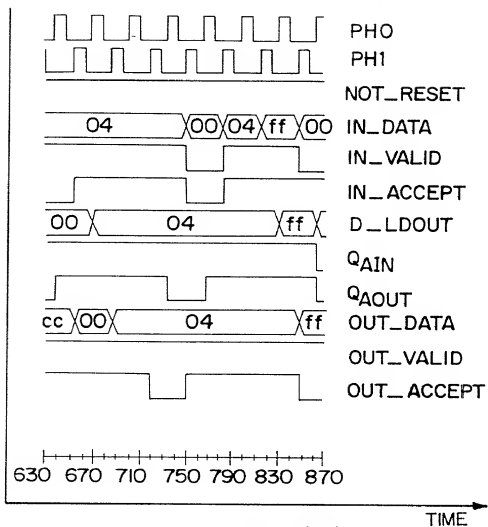


FIG. 5(B)

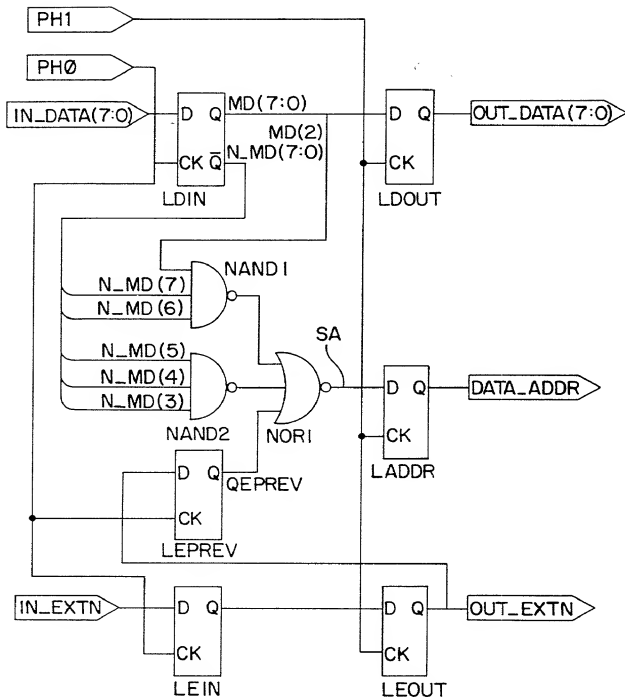
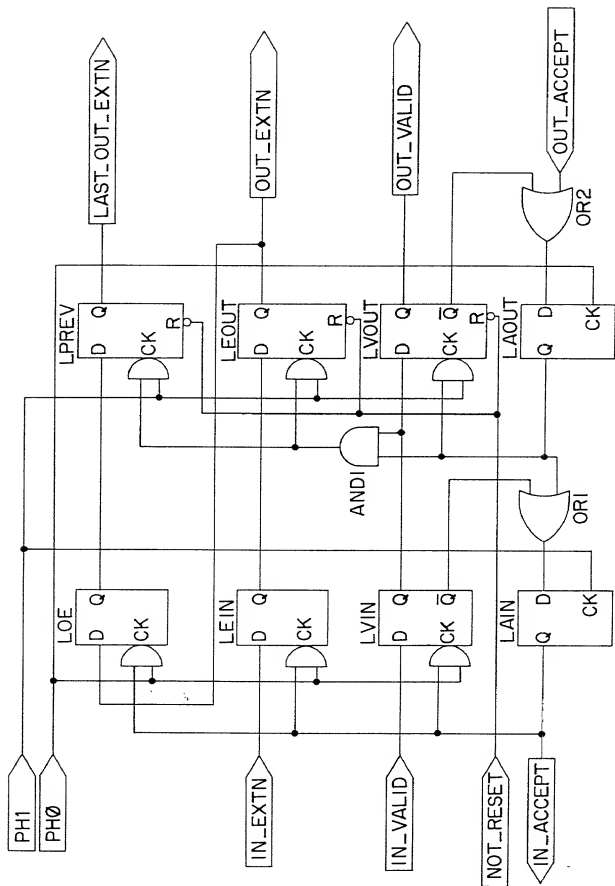


FIG. 6



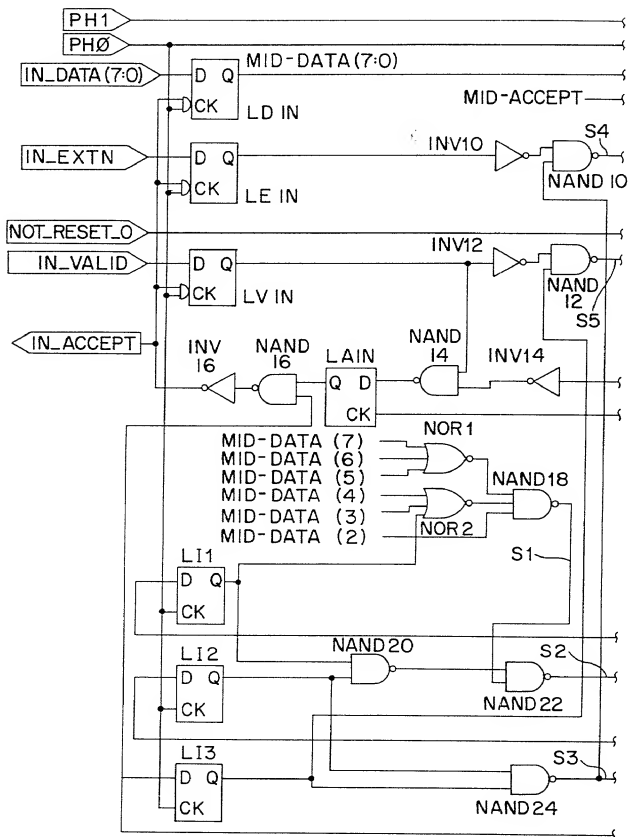


FIG. 8(A)

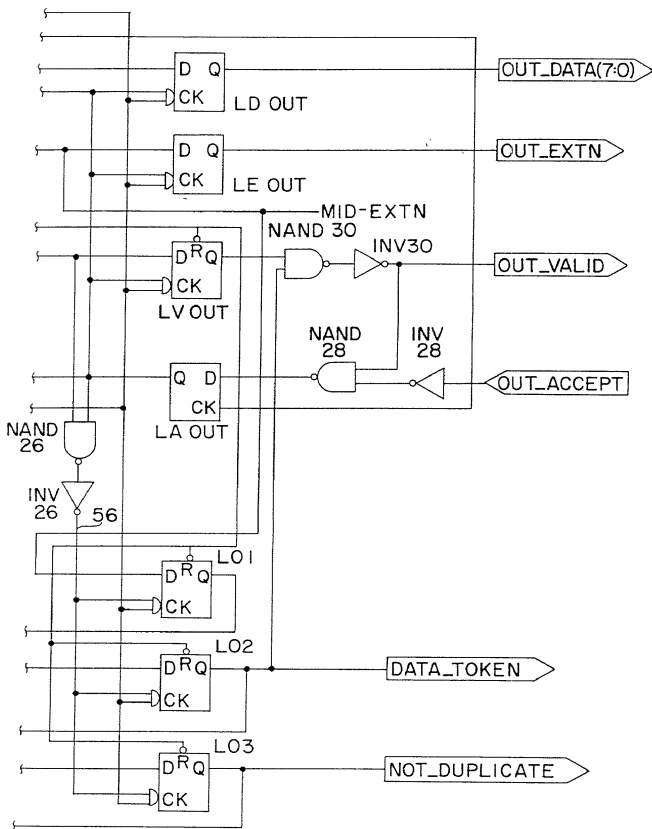


FIG. 8(B)

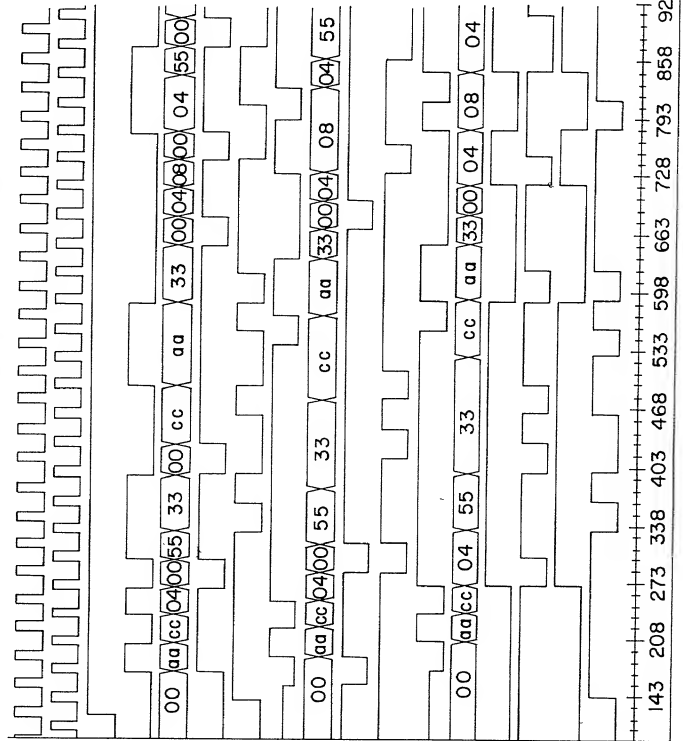


FIG. 9(A)

TIME

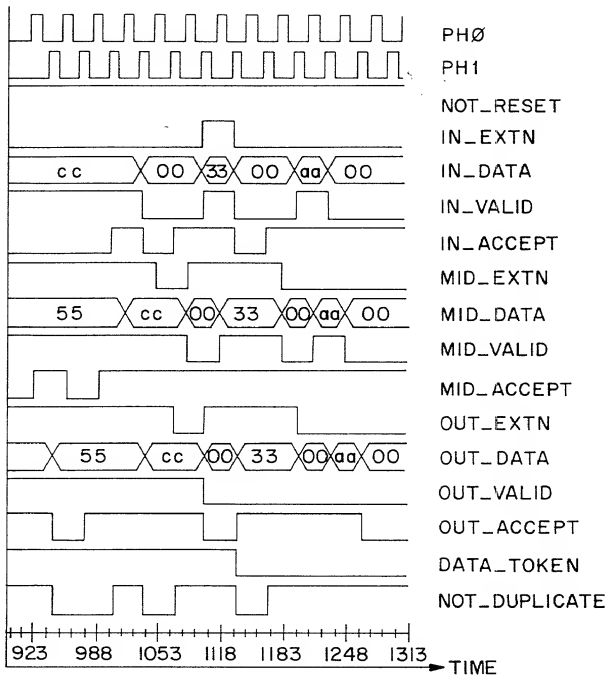


FIG. 9(B)

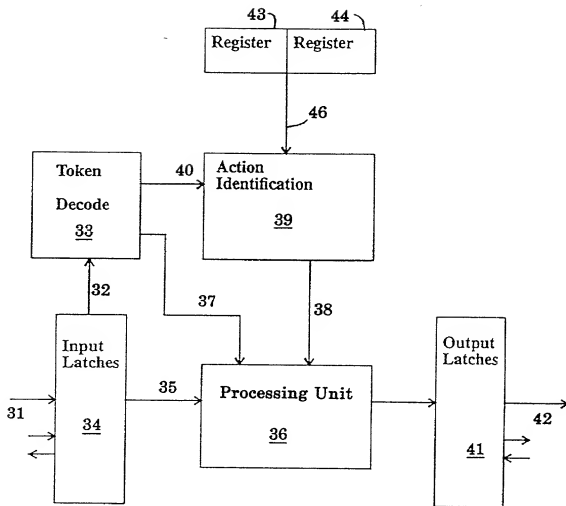


FIG. 10

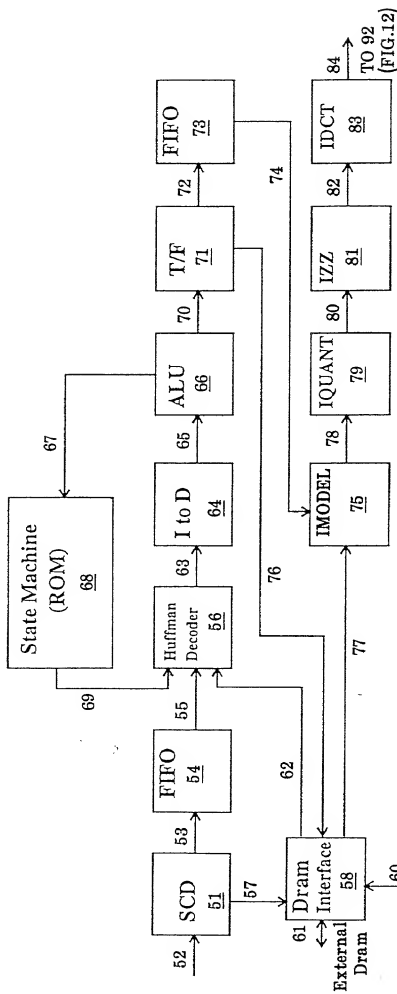


FIG. 11

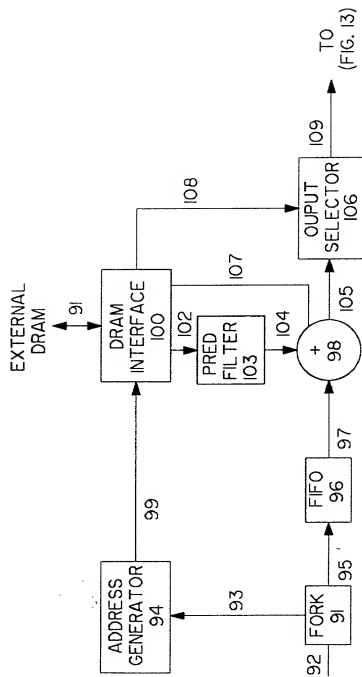


FIG. 12

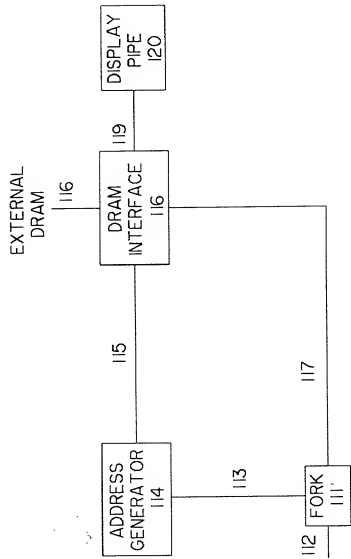


FIG. 13

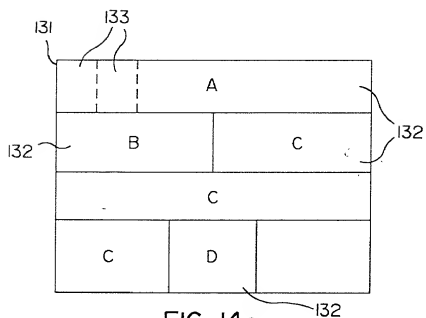


FIG. 14a

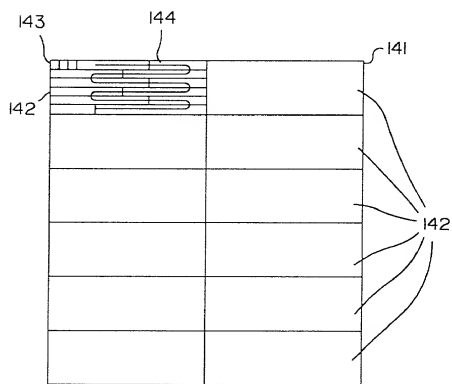


FIG. 14b

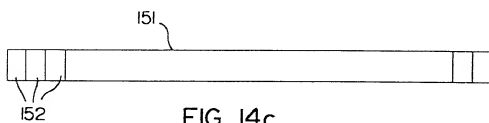


FIG. 14c

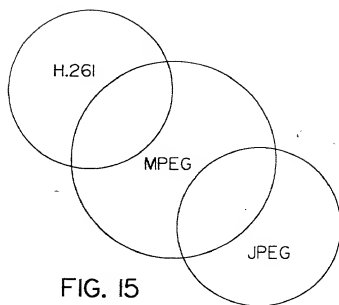


FIG. 15

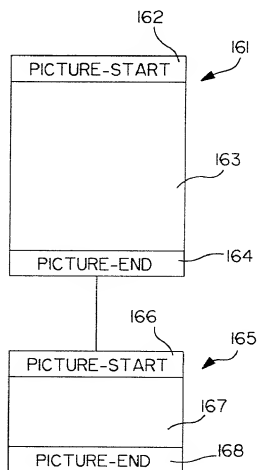


FIG. 16

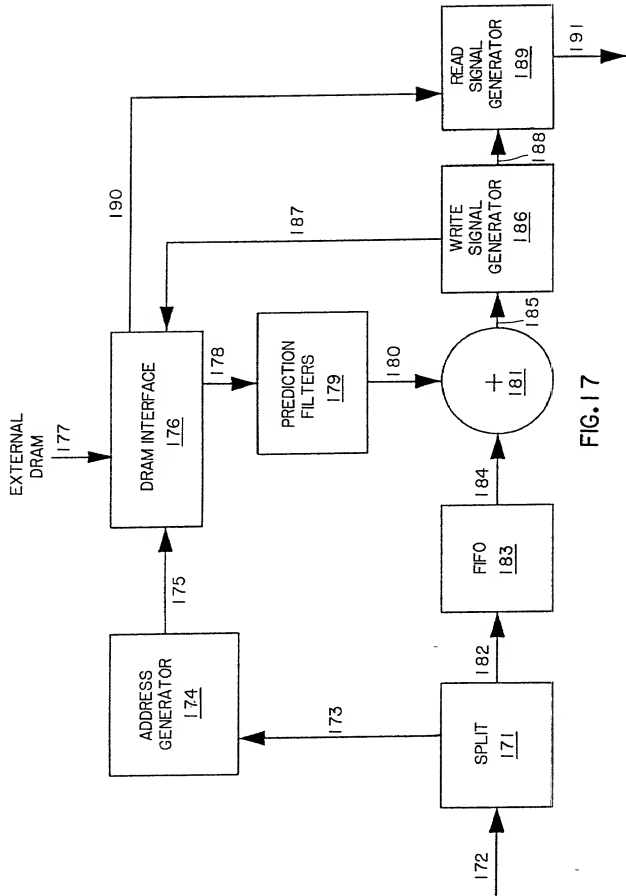


FIG. 17

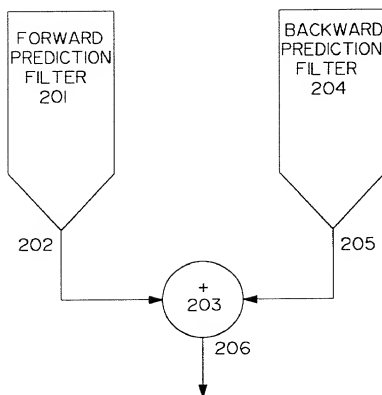


FIG. 18

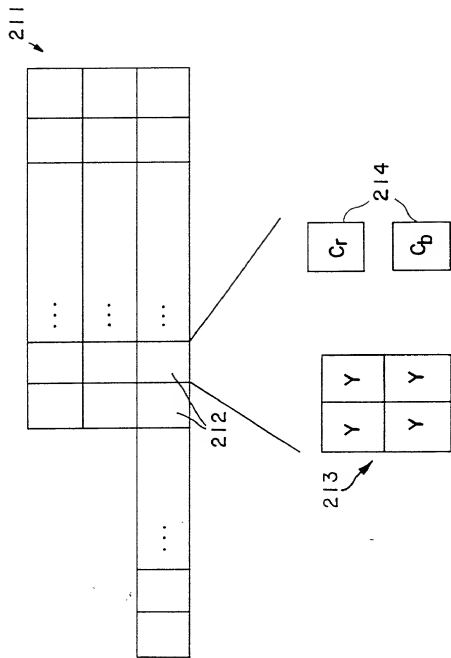


FIG. 19

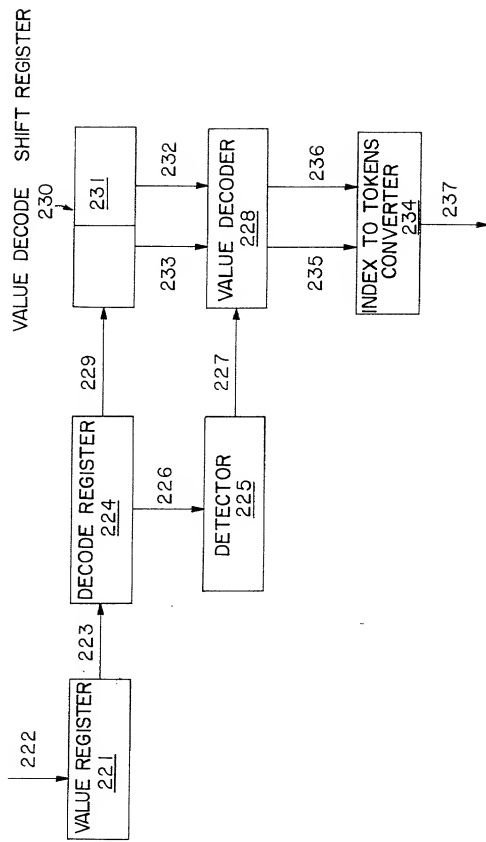


FIG. 20

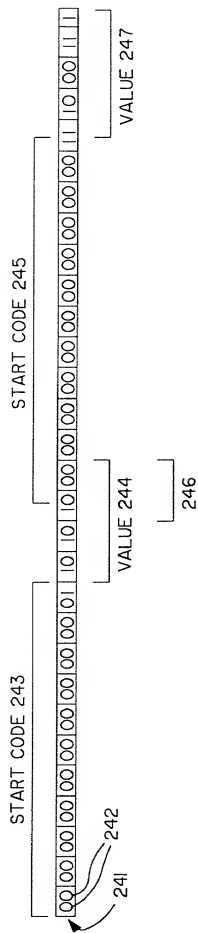


FIG. 21

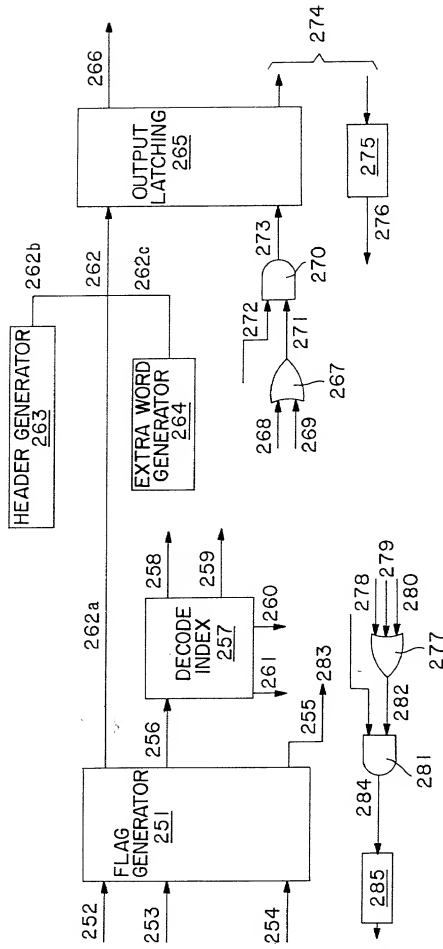


FIG. 22

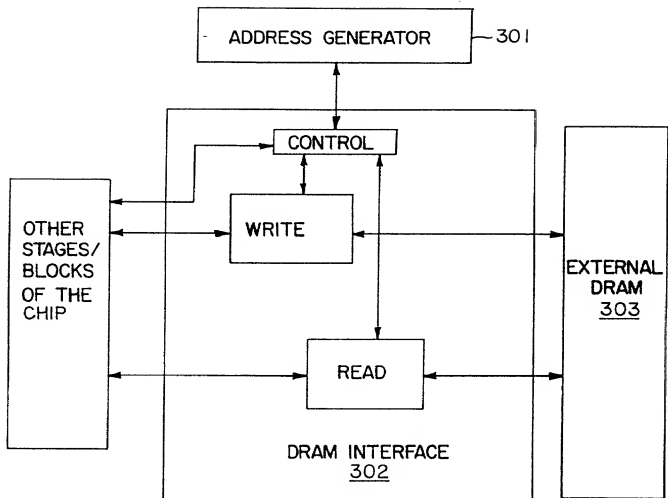


FIG.23

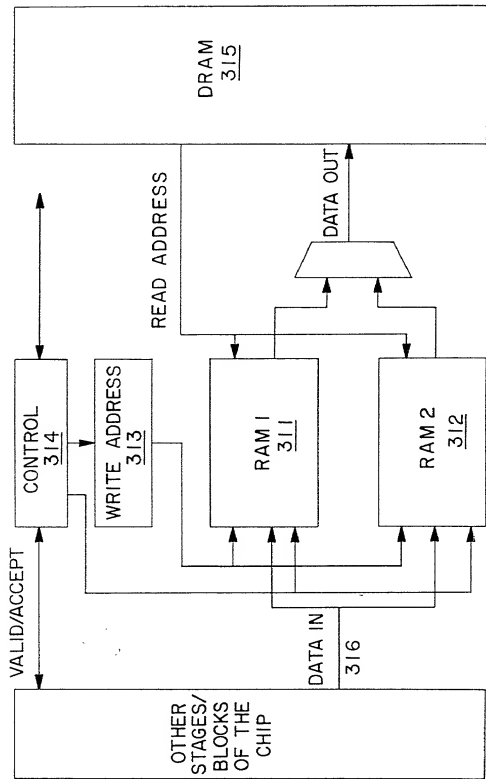


FIG.24

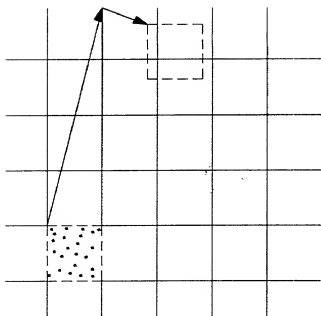


FIG. 25

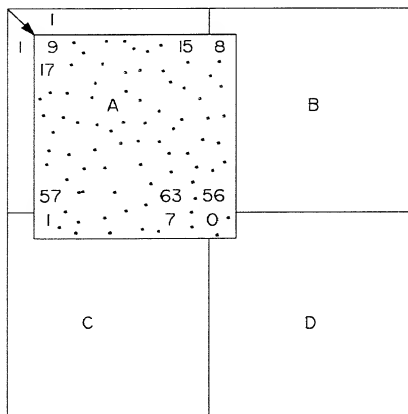


FIG. 26

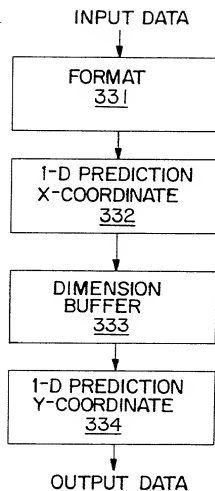


FIG.28

Multiplexed audio/video
data

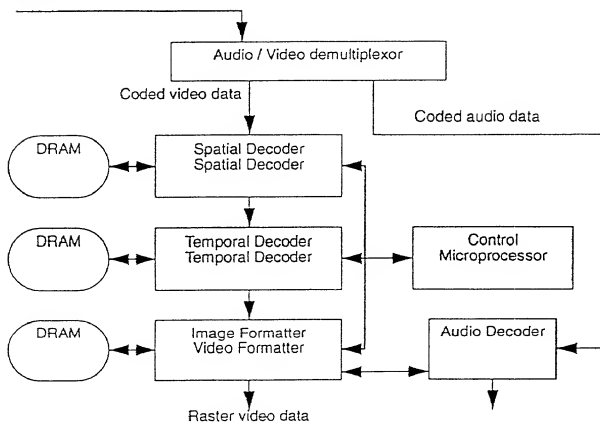


FIG.29

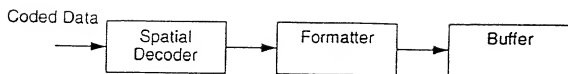


FIG.30

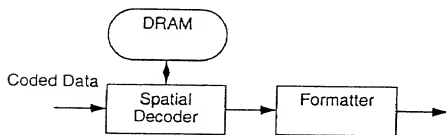


FIG.31

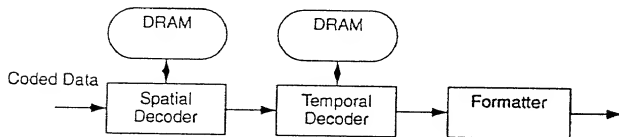


FIG.32

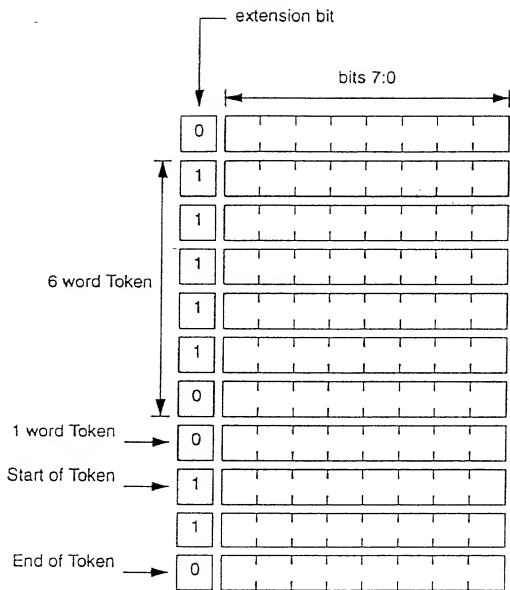


FIG.33

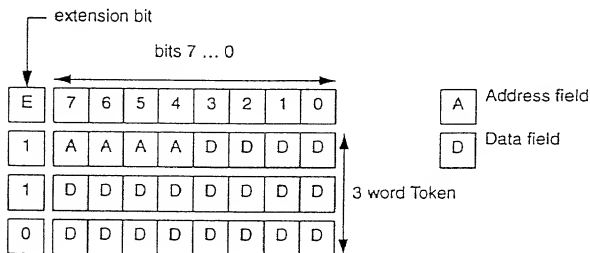


FIG.34

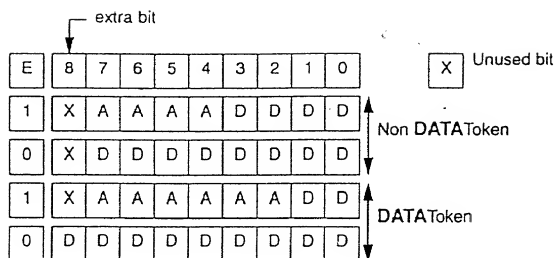
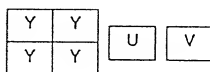
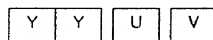


FIG.35



MPEG 4:2:0
macroblock

FIG.36A



JPEG 2:1:1
macroblock

FIG.36B

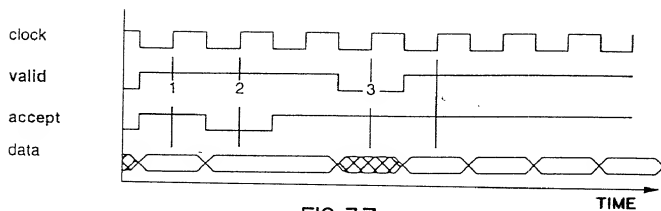


FIG.37

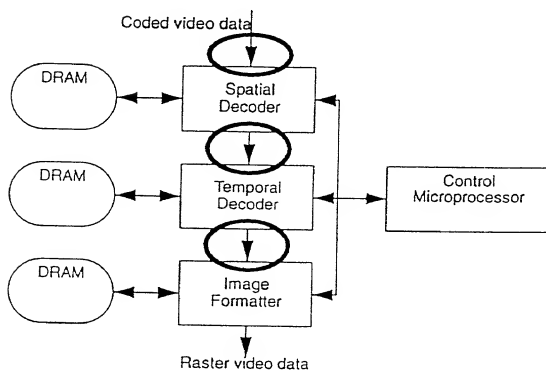


FIG.38

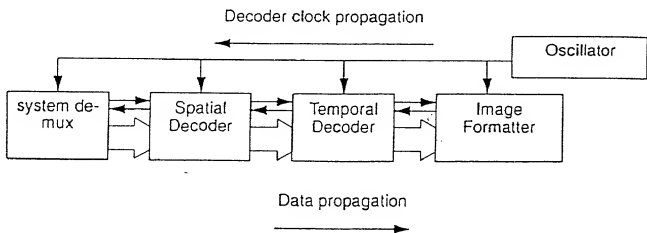


FIG.39

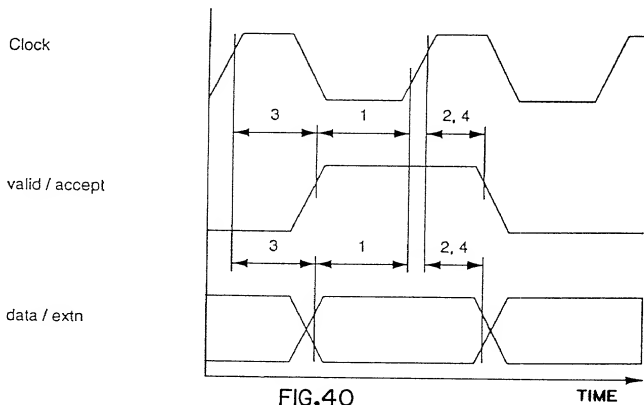


FIG.40



FIG.41

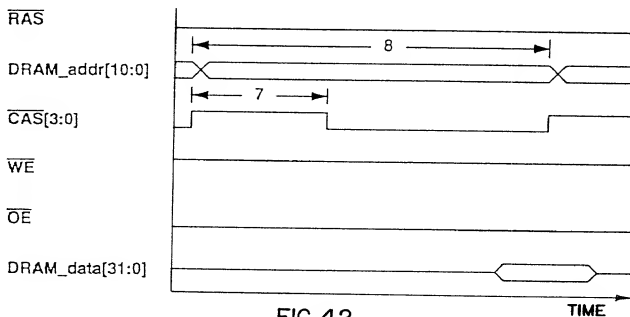


FIG.42

The diagram illustrates the timing for a DRAM refresh operation. It is divided into three main sections:

- Row address timing:** Shows the RAS signal (active low) and the DRAM address [10:0]. The RAS signal is active for a duration of 5. The WE signal (active low) is also shown.
- Start of read:** Shows the CAS [3:0] signal (active low), the OE signal (active low), and the data [31:0] signal. The CAS signal is active for a duration of 6. The data signal is shown as a read operation.
- Start of write:** Shows the CAS [3:0] signal (active low), the OE signal (active low), and the data [31:0] signal. The CAS signal is active for a duration of 7. The data signal is shown as a write operation.

The horizontal axis represents TIME.

TIME

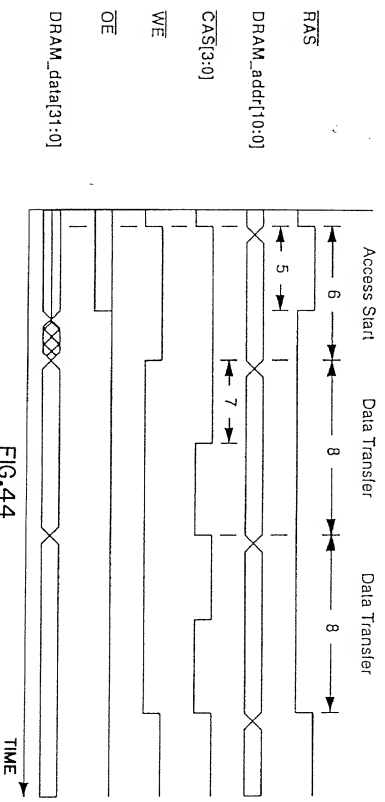


FIG.44

RAS

DRAM_addr[10:0]

$\overline{\text{CAS}}[3:0]$

WE

 \overline{OE}

DRAM_data[31:0]

FIG.45

RAS

DRAM_addr[10:0]

 $\overline{\text{CAS}}[3:0]$

WE

 \overline{OE}

DRAM_data[31:0]

FIG.46

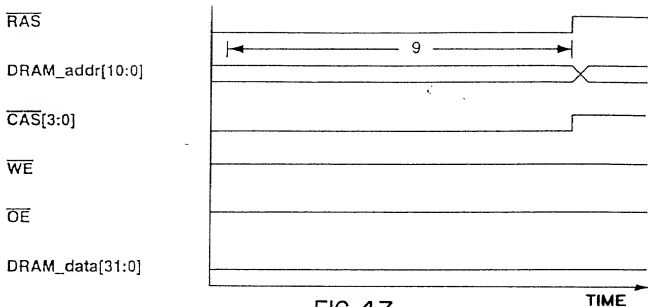


FIG.47

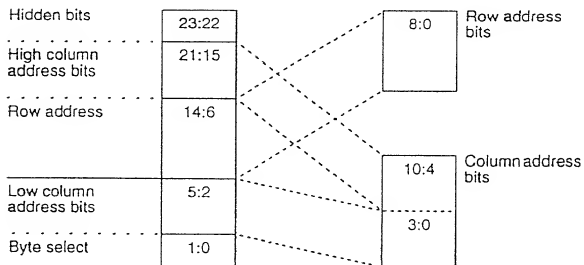


FIG.48

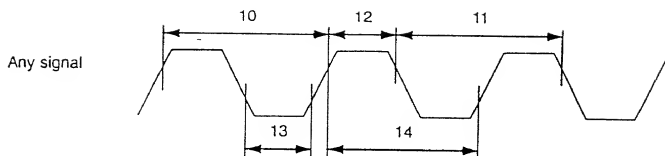


FIG.49

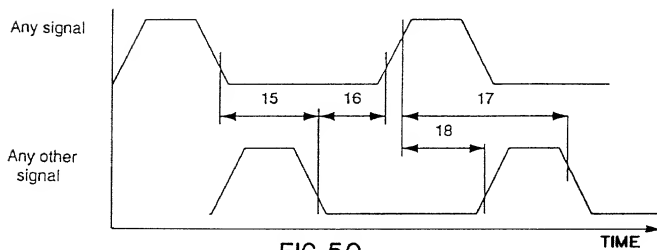
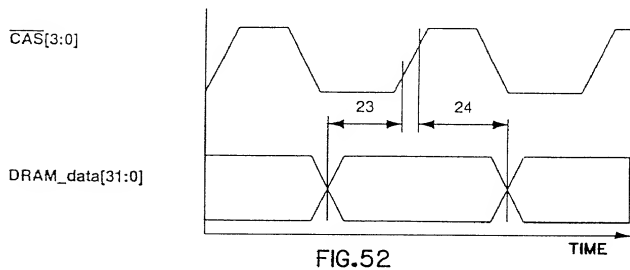
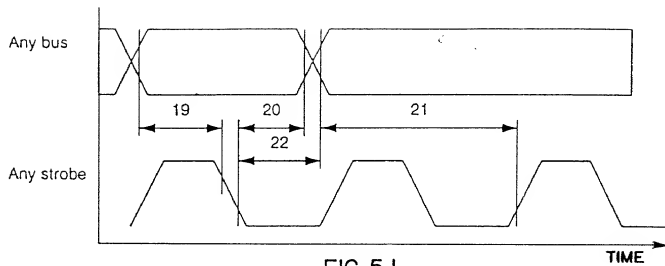


FIG.50



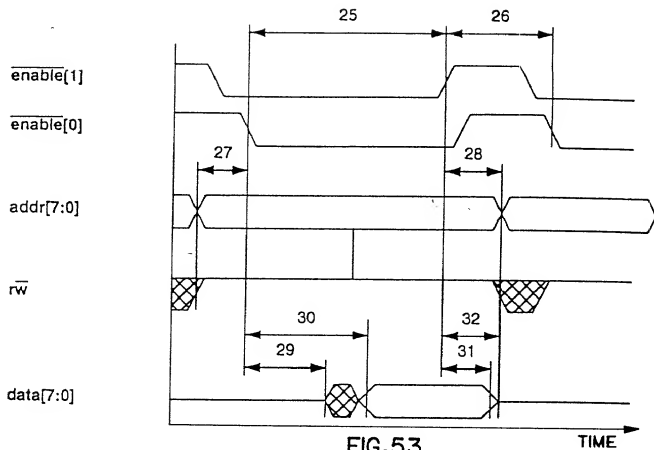


FIG.53

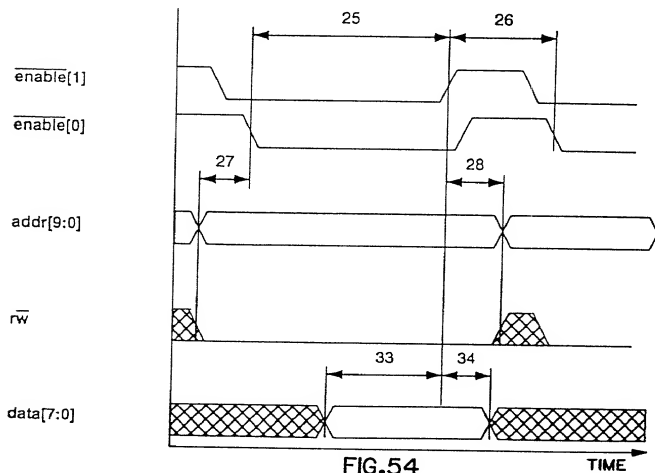


FIG.54

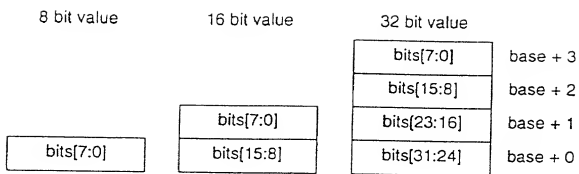


FIG.55

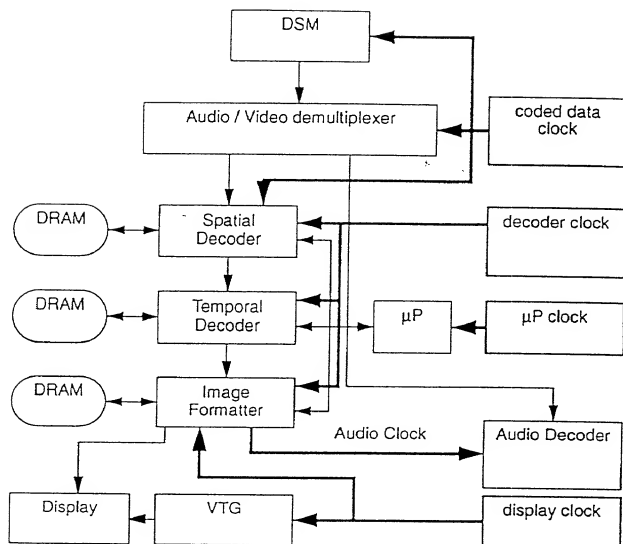


FIG.56

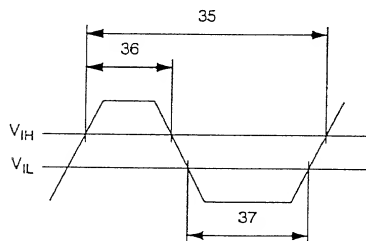


FIG.57

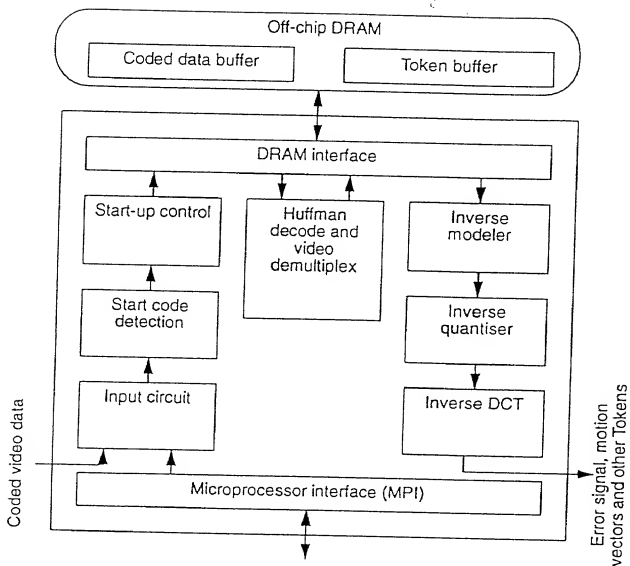


FIG.58

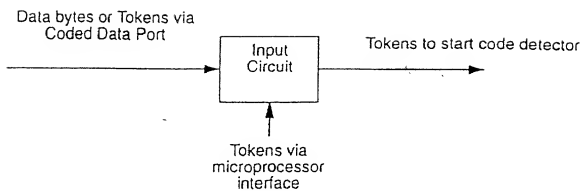


FIG.59

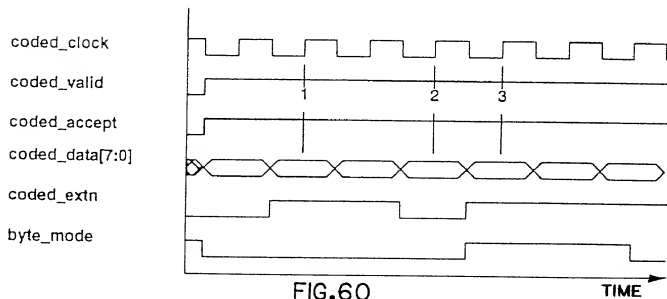


FIG.60

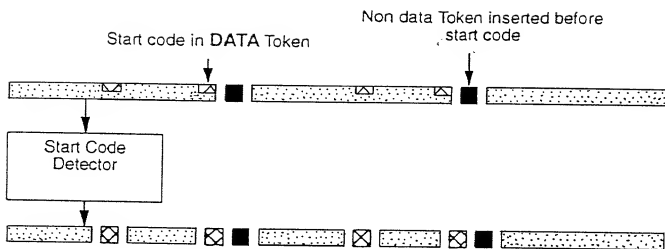


FIG.63

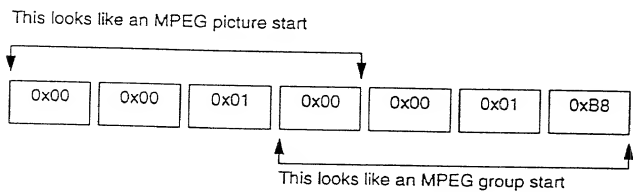


FIG.64

This looks like an MPEG slice start (0x28)

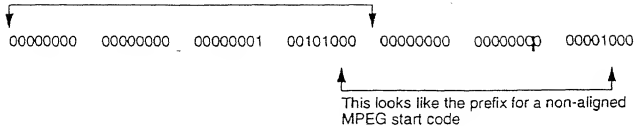


FIG.65

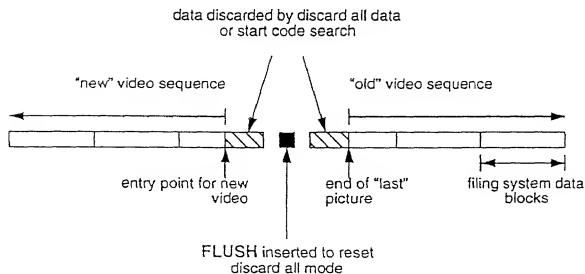


FIG.66

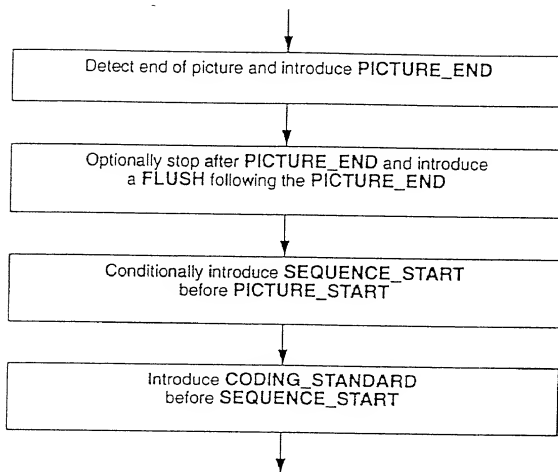


FIG.67

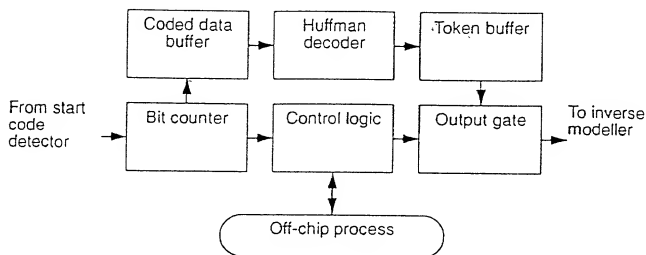


FIG. 68

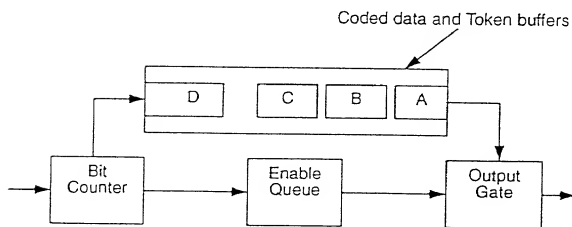


FIG. 69

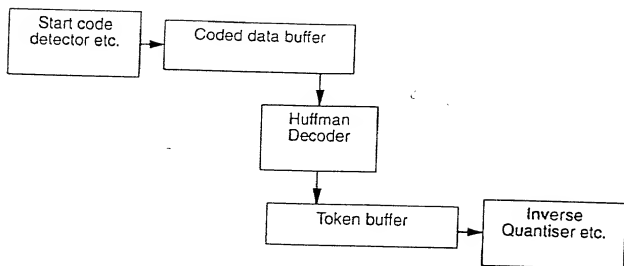


FIG.70

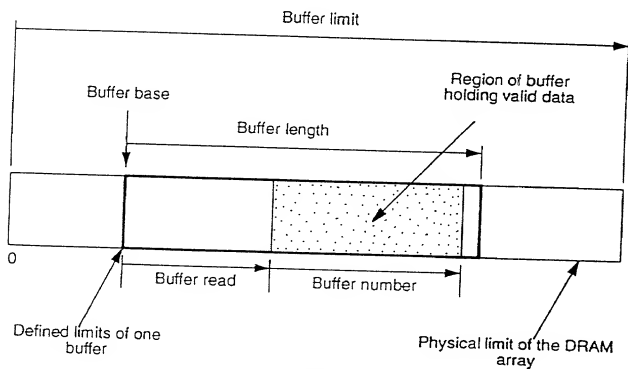


FIG.71

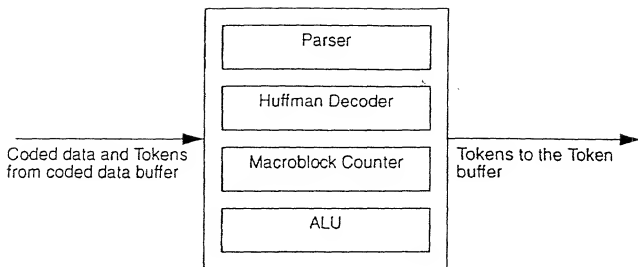


FIG.72

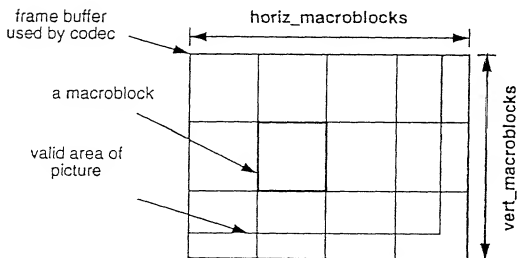


FIG.73

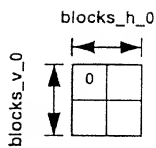


FIG.74A

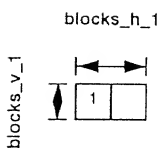


FIG.74B

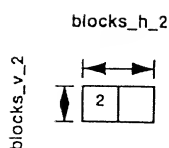


FIG.74C

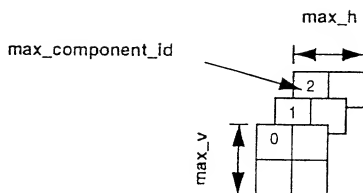


FIG.74D

$$\left\{ \begin{array}{l} \text{horiz_macroblocks} = \frac{\text{horiz_pels} + 15}{16} \\ \text{vert_macroblocks} = \frac{\text{vert_pels} + 15}{16} \end{array} \right.$$

FIG.75

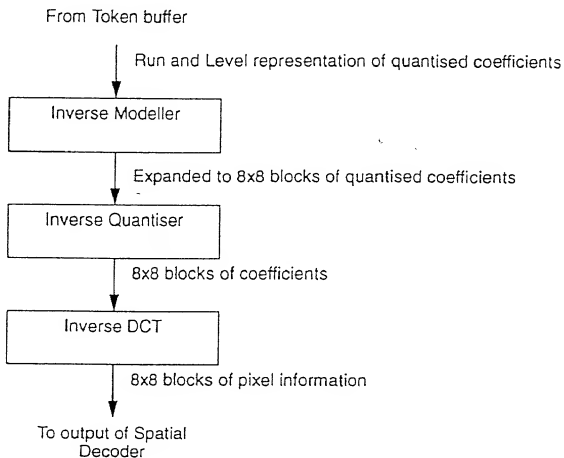


FIG.76

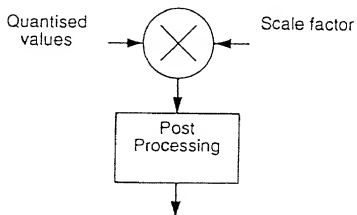


FIG.77

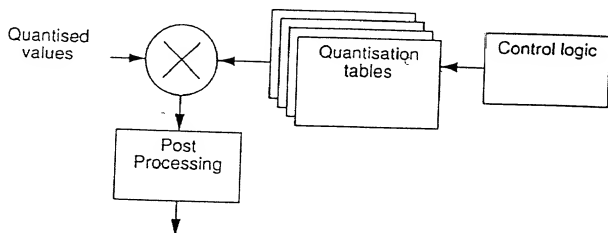


FIG.78

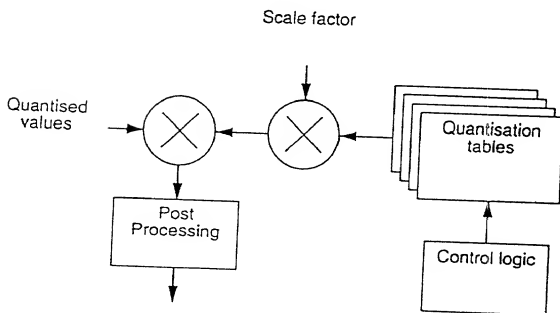


FIG.79

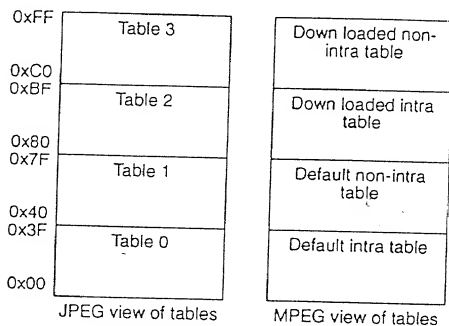


FIG.80

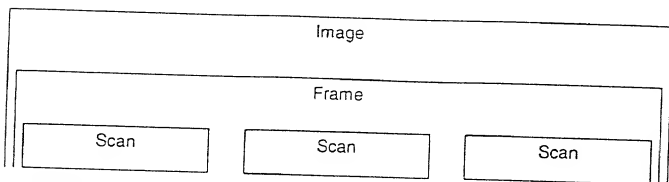


FIG.81

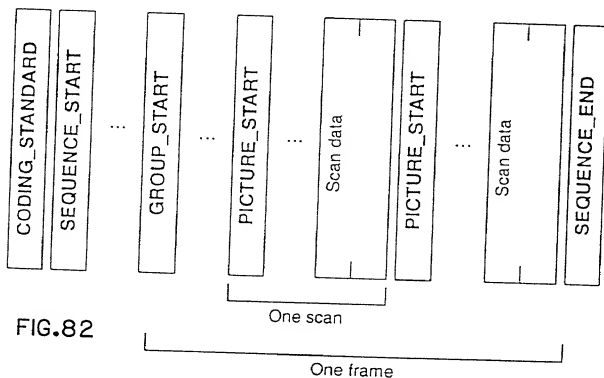


FIG.82

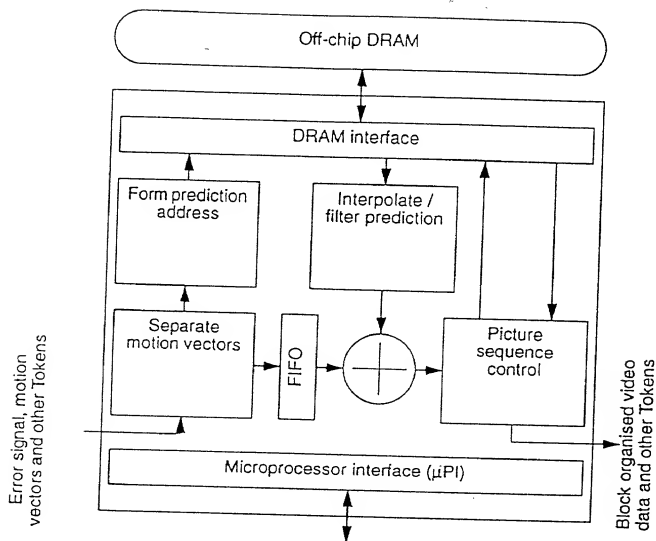


FIG.83

The diagram illustrates a video stream structure with a vertical buffer. The buffer is divided into six horizontal slots. The top two slots are for Picture 1 (Component 2 and Component 1), and the bottom two slots are for Picture 0 (Component 2 and Component 1). The middle two slots are for Picture 1 (Component 0 and Component 1). The buffer is labeled 'picture_buffer_1' on the left. On the right, arrows indicate the offsets for each component: 'component_offset_2' for the top two slots, 'component_offset_1' for the middle two slots, and 'component_offset_2' for the bottom two slots. The buffer is also labeled 'picture_buffer_0' on the left.

Picture's temporal reference → 0 3 1 2 6 4 5

Picture sequence in coded data

0 1 2 3 4 5 6

Picture sequence required for display

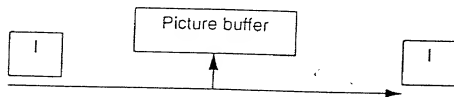


FIG. 86

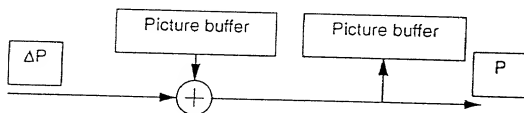


FIG. 87

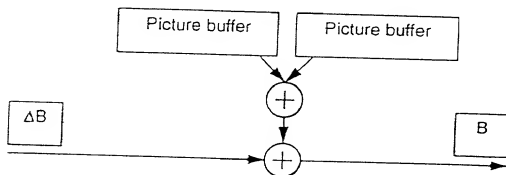
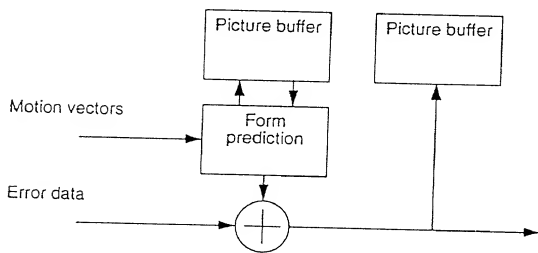


FIG. 88



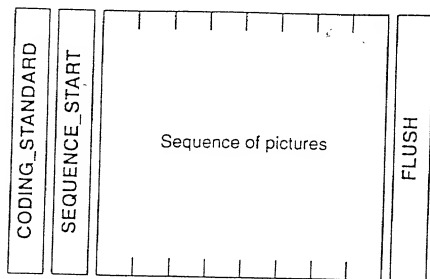


FIG.9 I

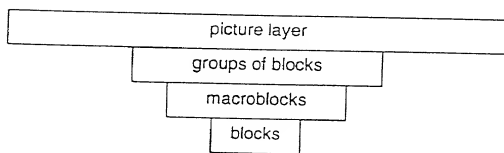


FIG.92

200910-0002760

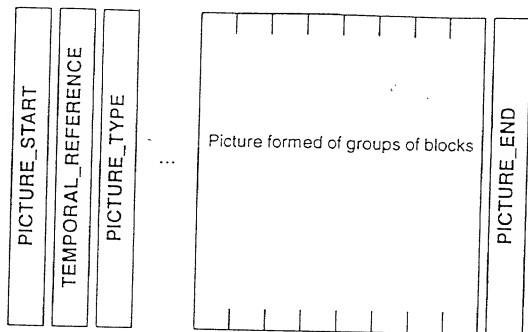


FIG.93

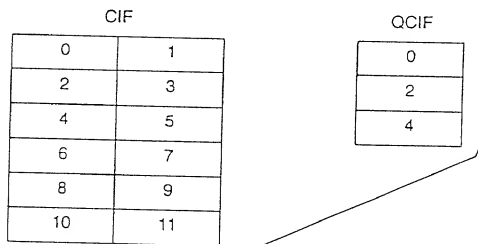


FIG.94

100510-9602/460

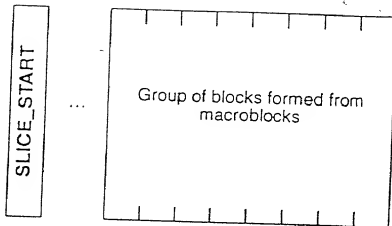


FIG.95

| | | | | | | | | | | |
|----|----|----|----|----|----|----|----|----|----|----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
| 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
| 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 |

FIG.96

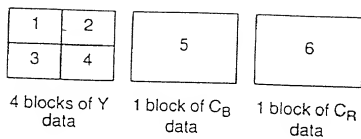


FIG.97

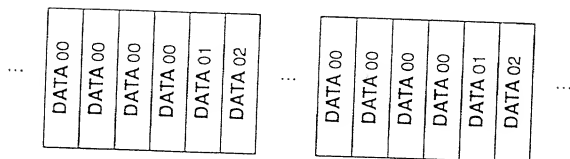


FIG.98

| | | | | | | | |
|---|----|----|----|----|----|----|----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |

⋮

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| 59 | 58 | 59 | 60 | 61 | 62 | 63 | 64 |
|----|----|----|----|----|----|----|----|

FIG.99

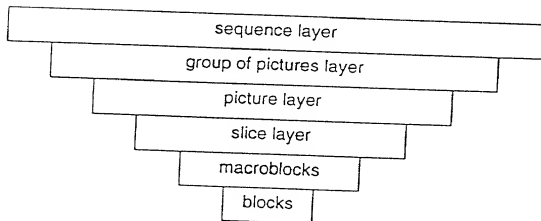


FIG. 100

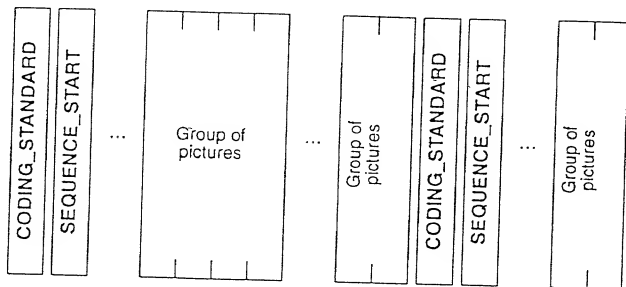


FIG. 101

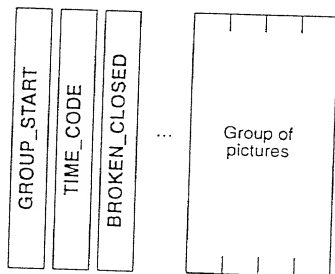


FIG. 102

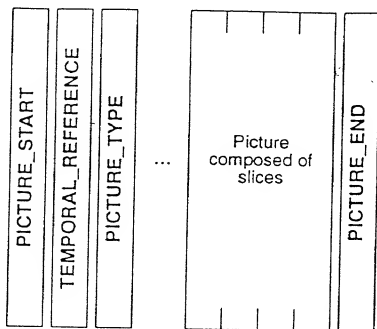


FIG. 103

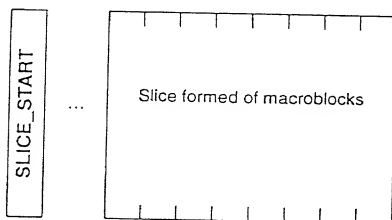


FIG. 104

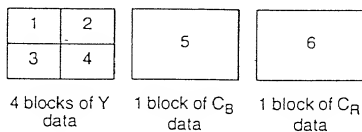


FIG. 105

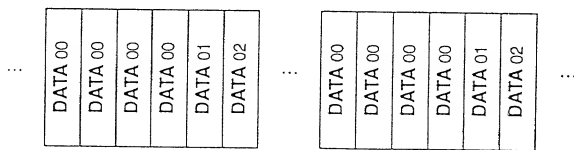


FIG. 106

FIG. 107

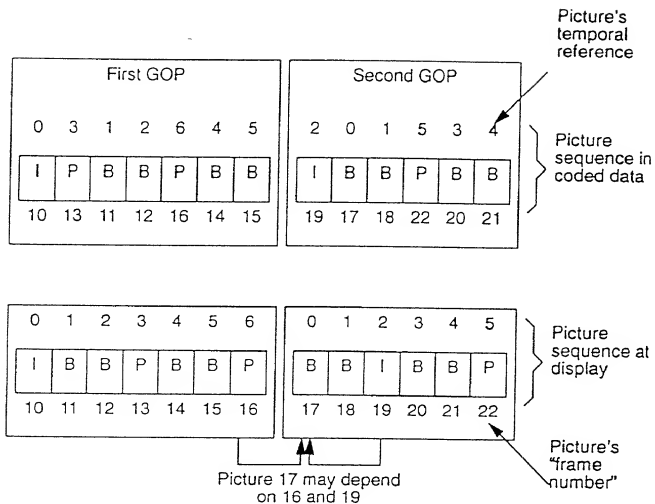


FIG. 107



FIG. 108

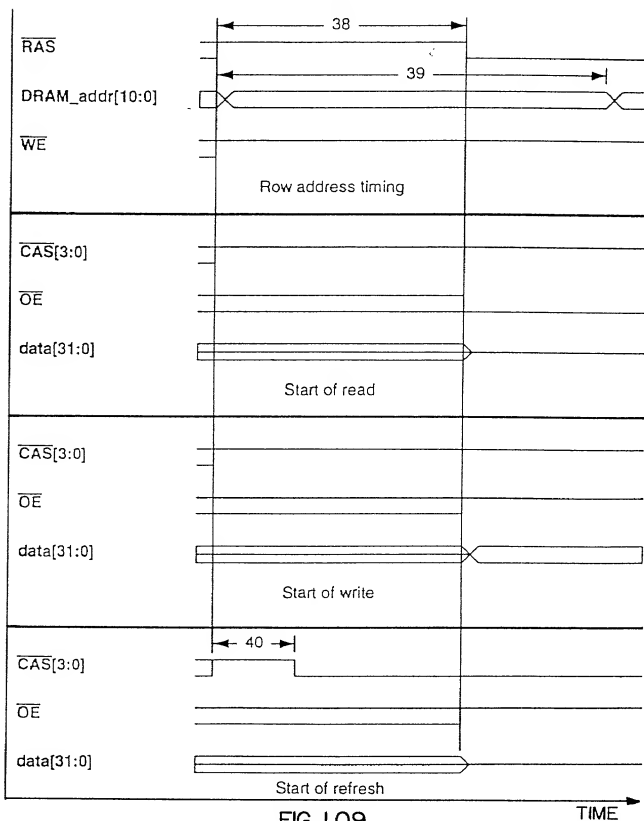


FIG. 109

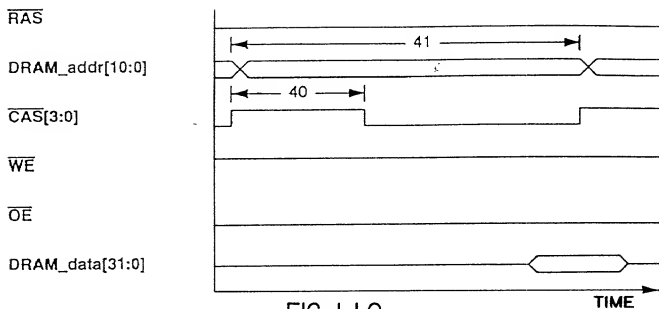


FIG. 110

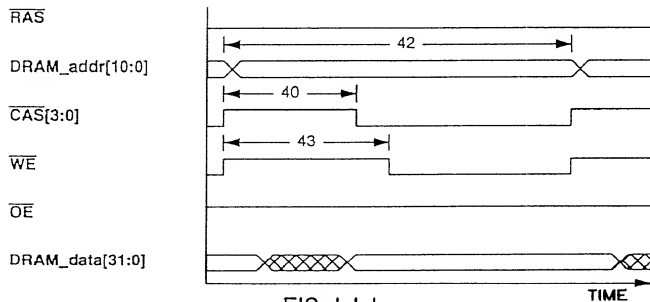


FIG. 111

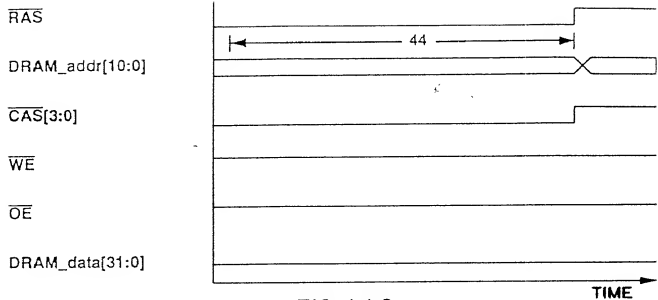


FIG. 1 | 2

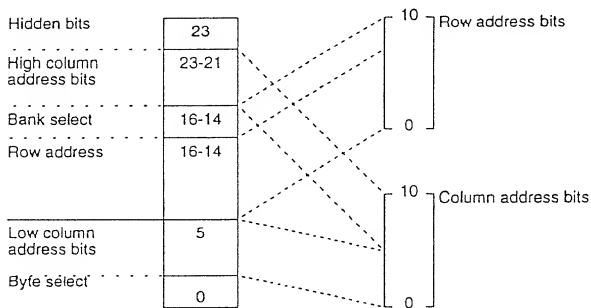


FIG. 1 | 3

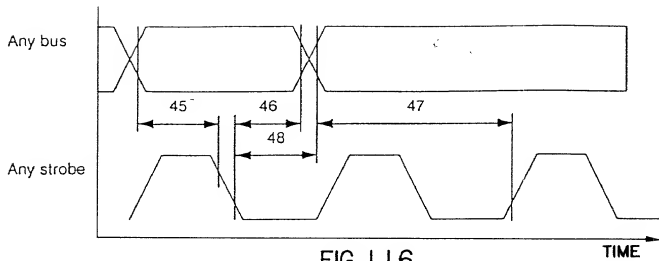


FIG. 116

CAS[3:0]

DRAM_data[31:0]

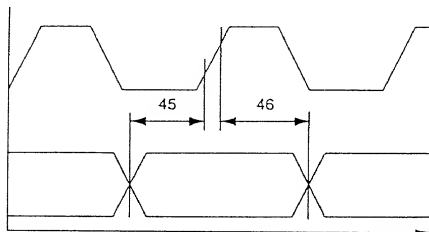


FIG. 117

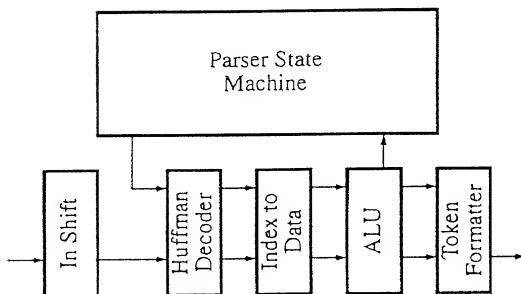


FIG. 118

FIG. 119

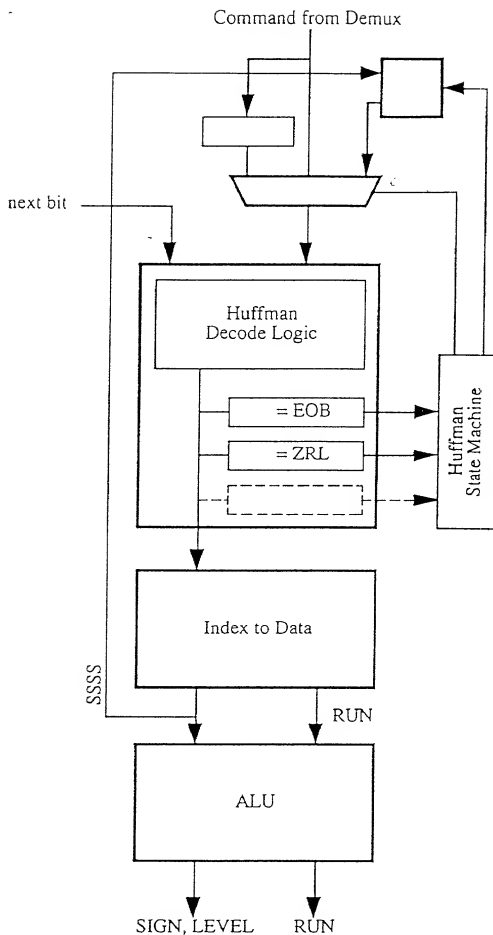


FIG. 120

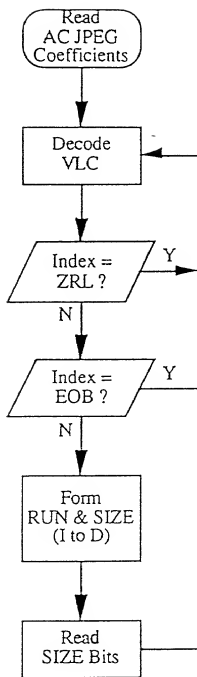


FIG. 121A

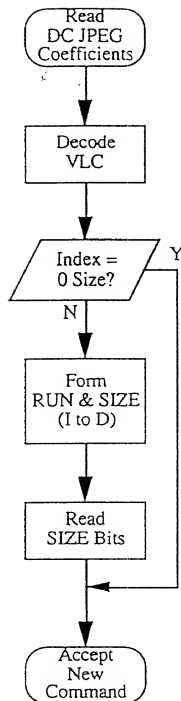


FIG. 121B

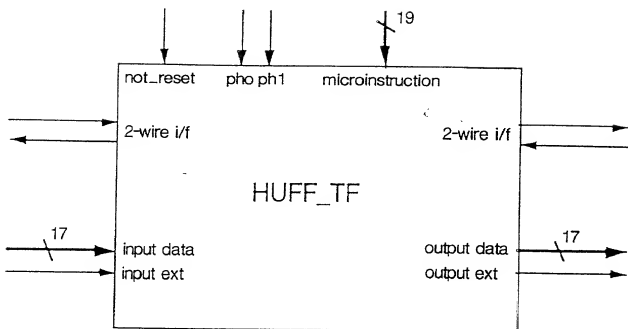


FIG. I 22

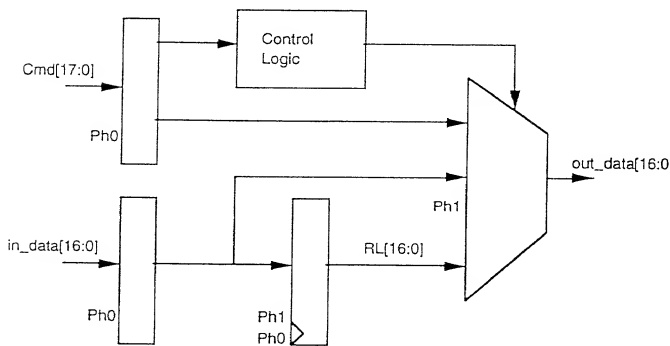


FIG. I 23

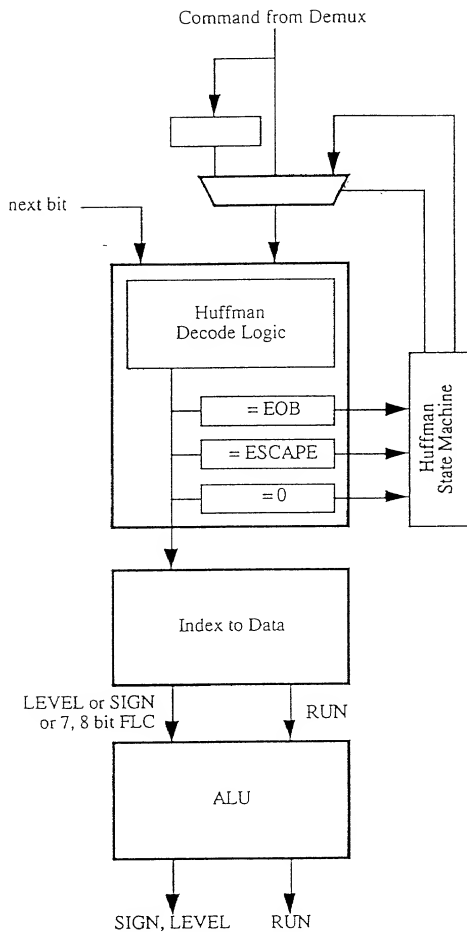


FIG. 124

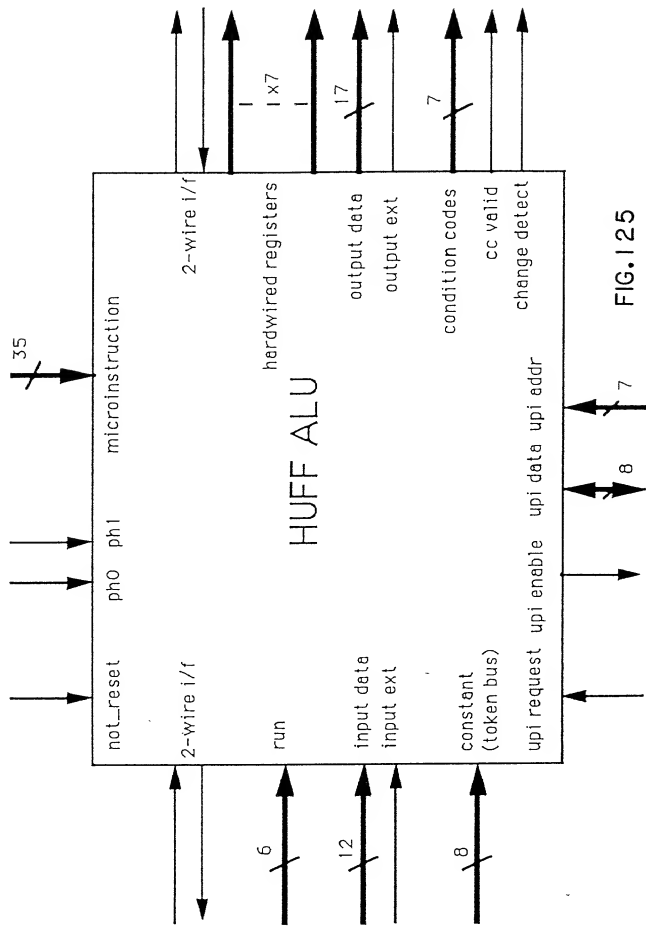


FIG. 125

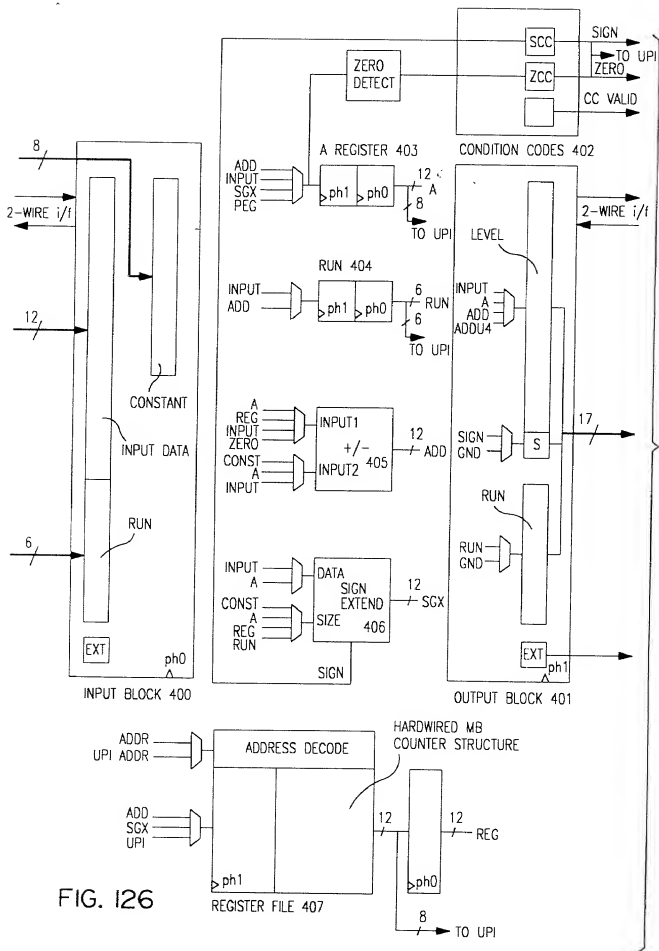


FIG. 126

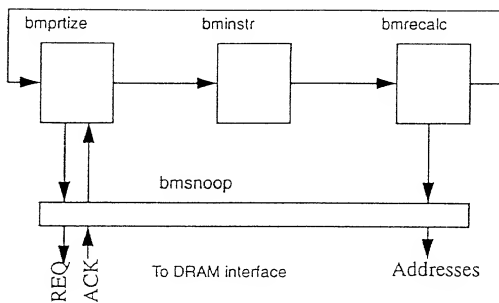


FIG. 127

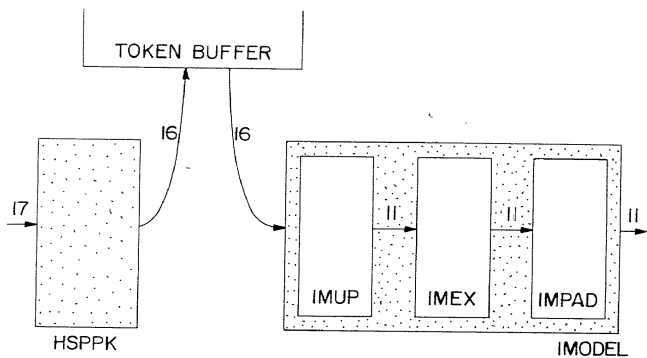


FIG. 128

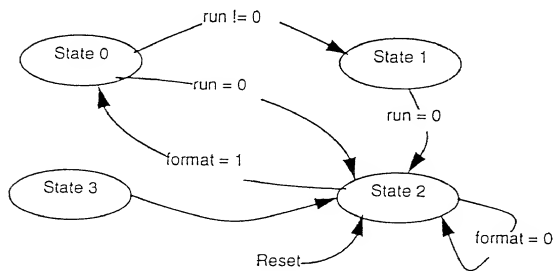


FIG. 129

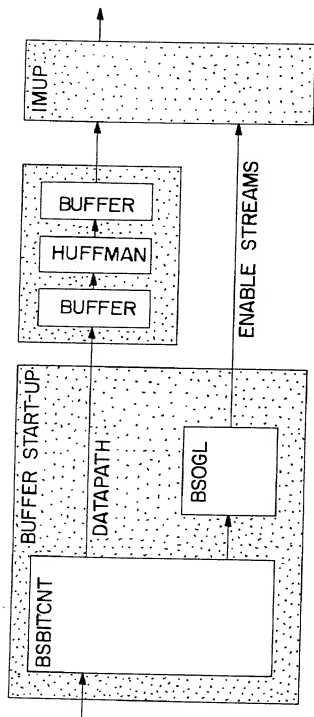


FIG. 130

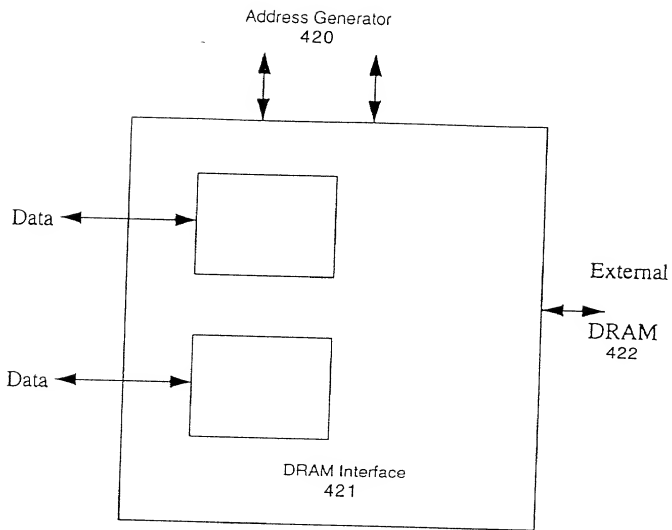


FIG. 131

The diagram illustrates a dual-port RAM architecture. At the top, a 'Control' block manages the system via a bidirectional 'valid/accept' signal. It provides a 'Write Address' to 'RAM 1' and a 'Read Address' to 'RAM 2'. A 4-bit 'Data In 430' bus is split into two 2-bit buses, each feeding into one of the RAM blocks. The outputs of both RAM blocks are combined into a 4-bit 'Data Out' bus.

FIG. 132

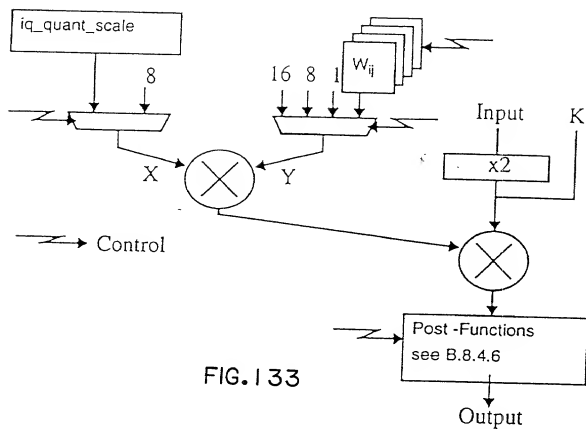


FIG. 133

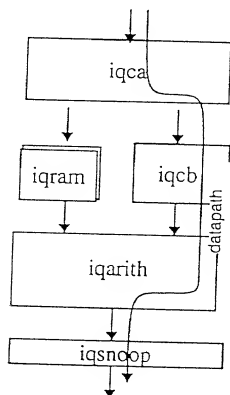


FIG. 134

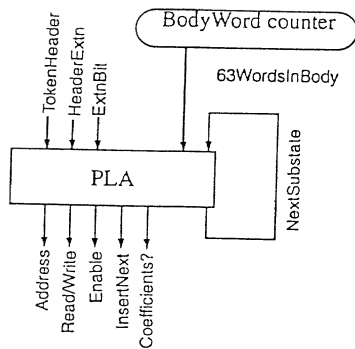


FIG. 135

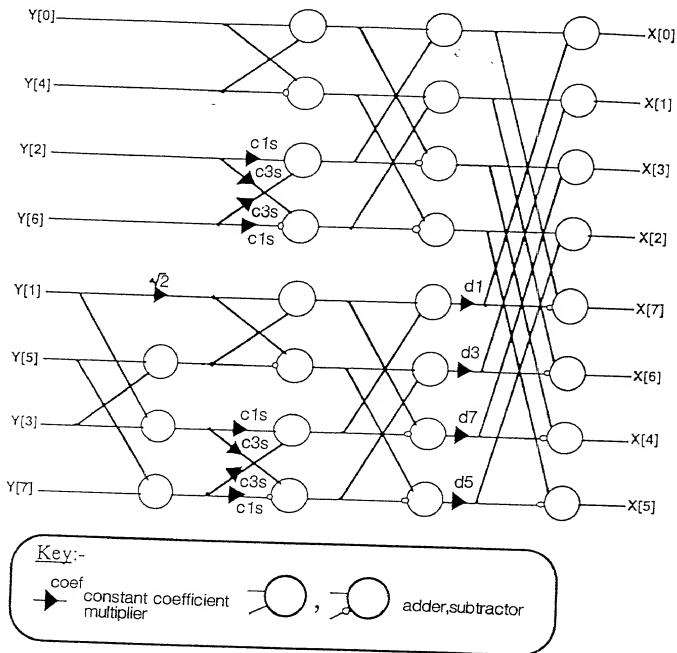
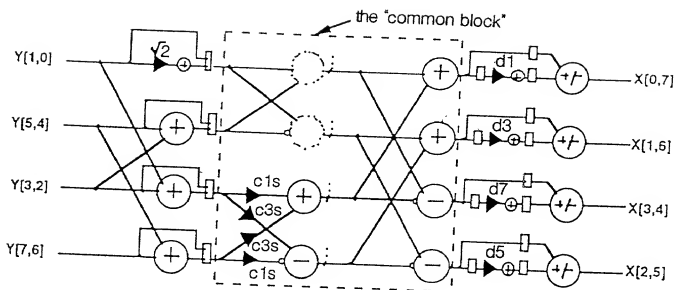


FIG. 136



Key:

- coef constant coefficient
- ➔ carry-save multiplier
- ⊗ multiplier output resolver
- ⊕ resolving adder, subtractor
- ⊕ resolving adder/subtractor

- ⊕, ⊖ carry-save adder, subtractor
- ⊕, ⊖ dummy adder/subtractor (combiners)
- ⌈ latch
- ⌈ 2-input mux latch

FIG. 137

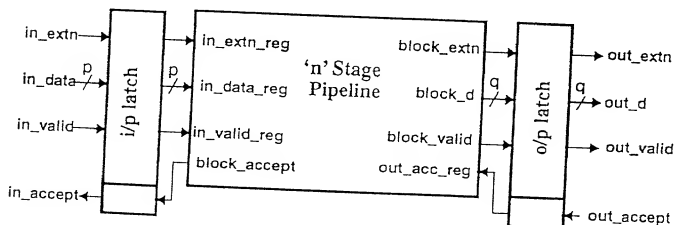


FIG. 138

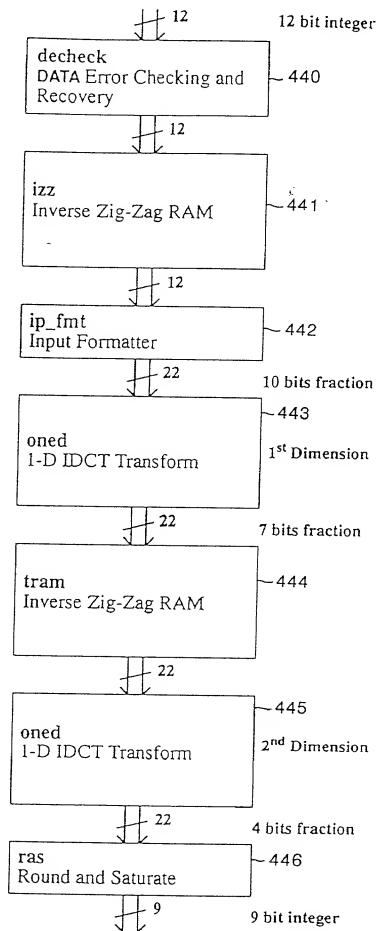


FIG. 139

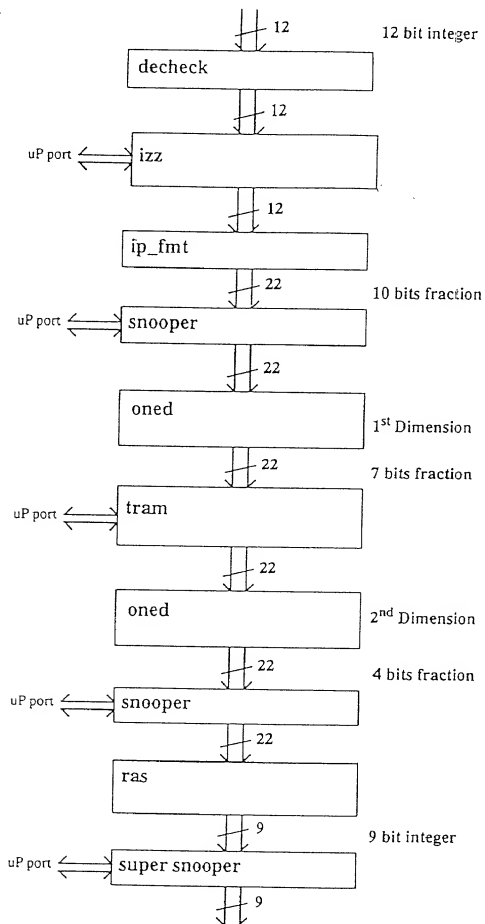


FIG. 140

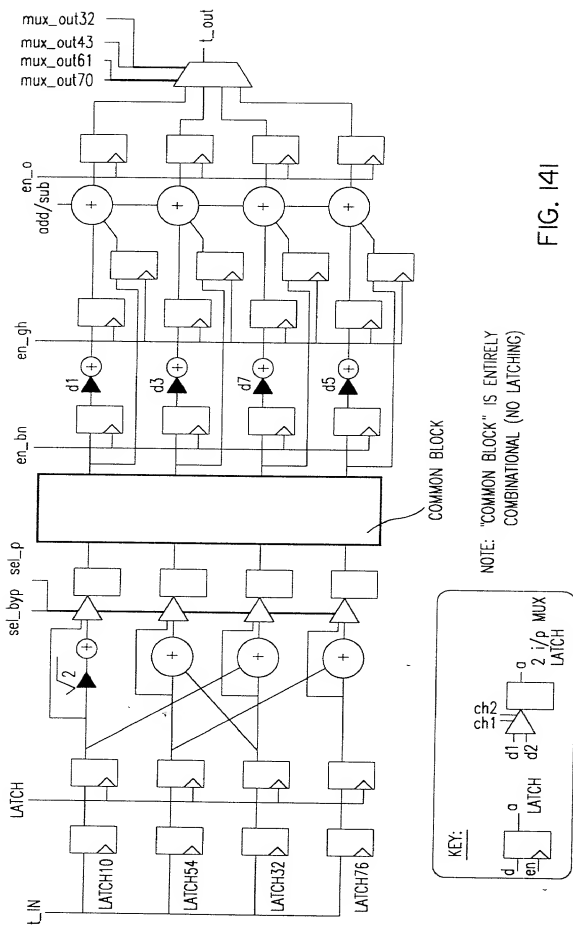


FIG. 141

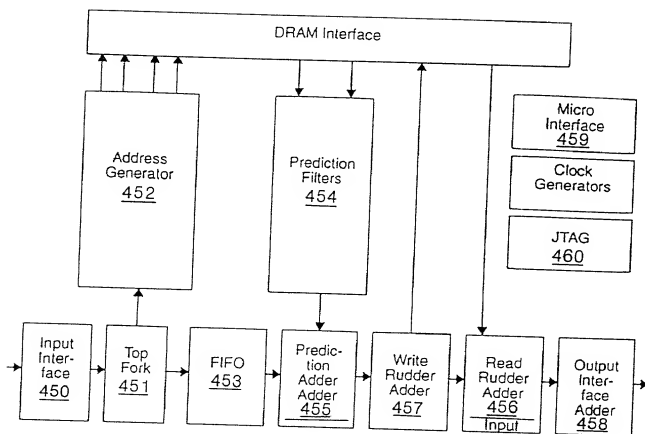


FIG. 142

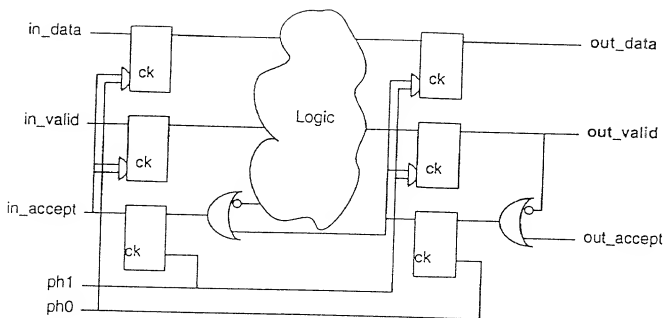


FIG. 143

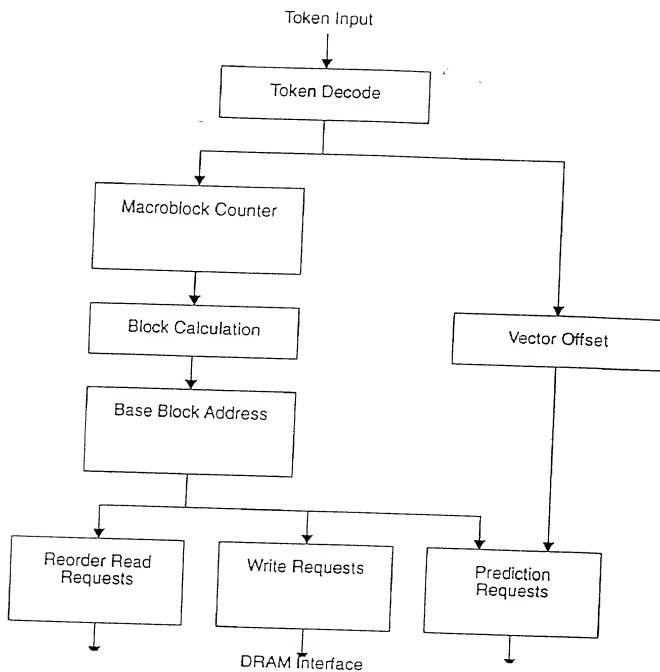


FIG. 144

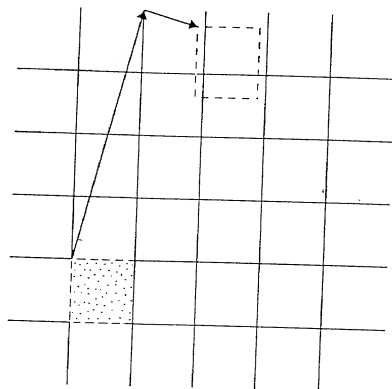


FIG. 145

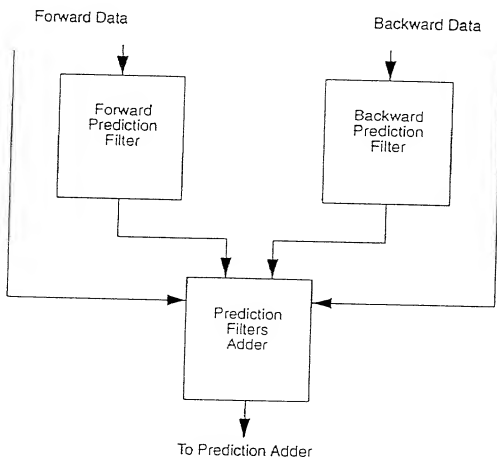


FIG. 146

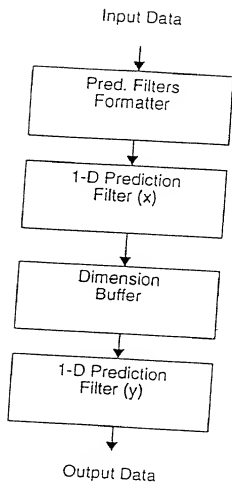


FIG. 1 47

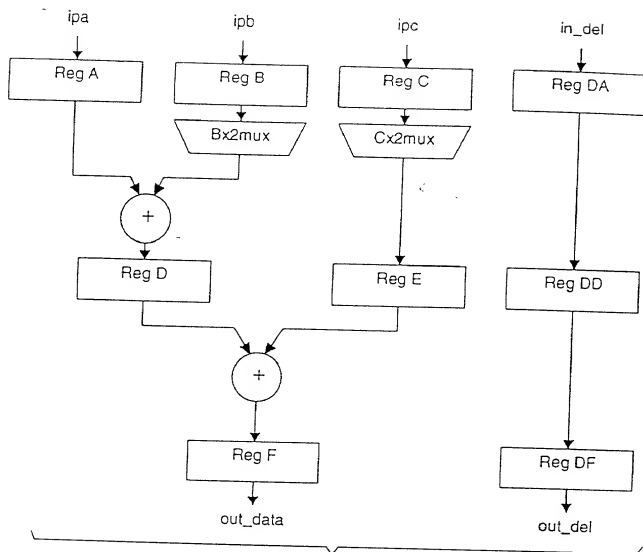


FIG. 148

| | | | | | | | |
|----|----|----|----|----|----|----|----|
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 |
| 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 |
| 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| 48 | 49 | 50 | 51 | 52 | 53 | 54 | 55 |
| 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |

FIG. 149

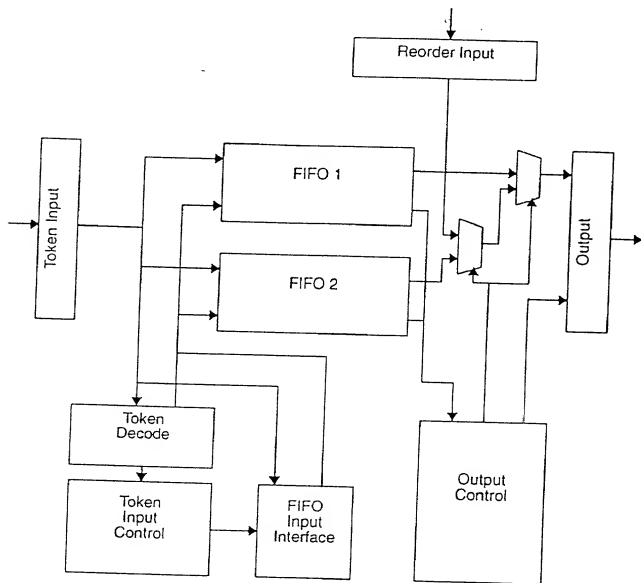


FIG. 1 50

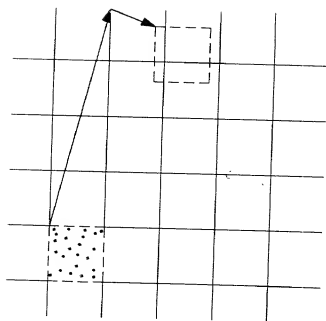


FIG. 151

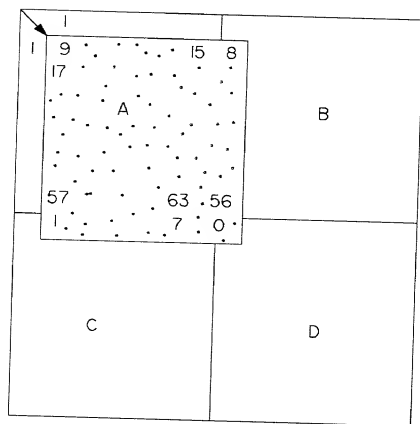


FIG. 152

Read Cycle

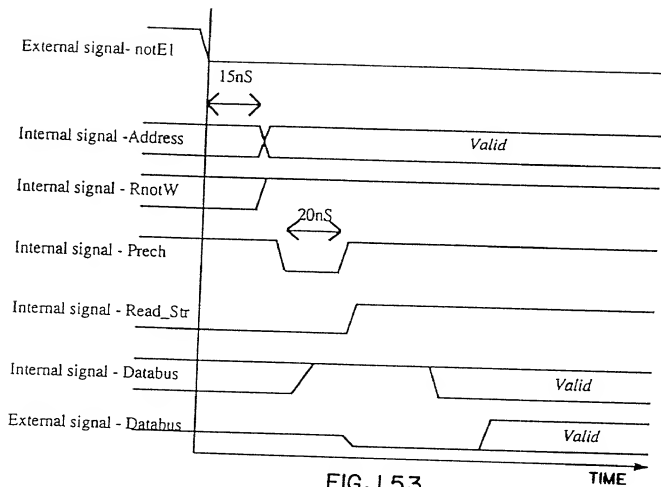


FIG. 153

Write Cycle

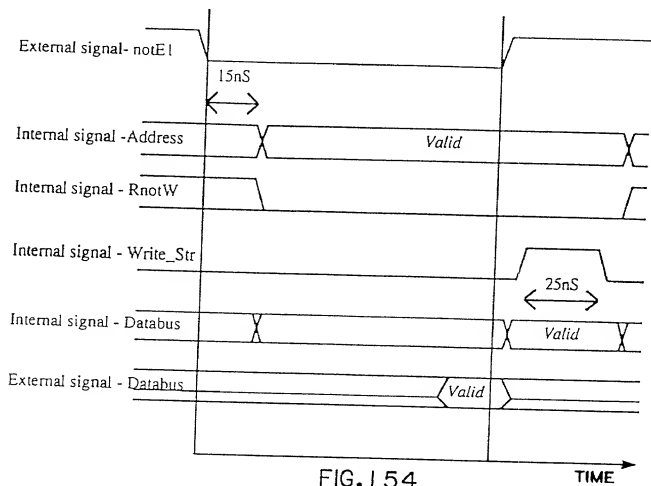


FIG. 154

TIME

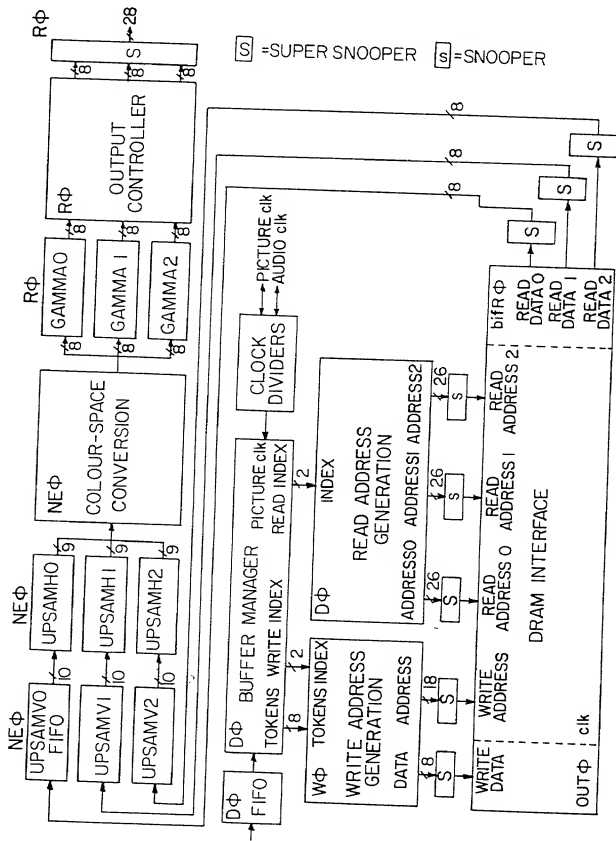


FIG. 155

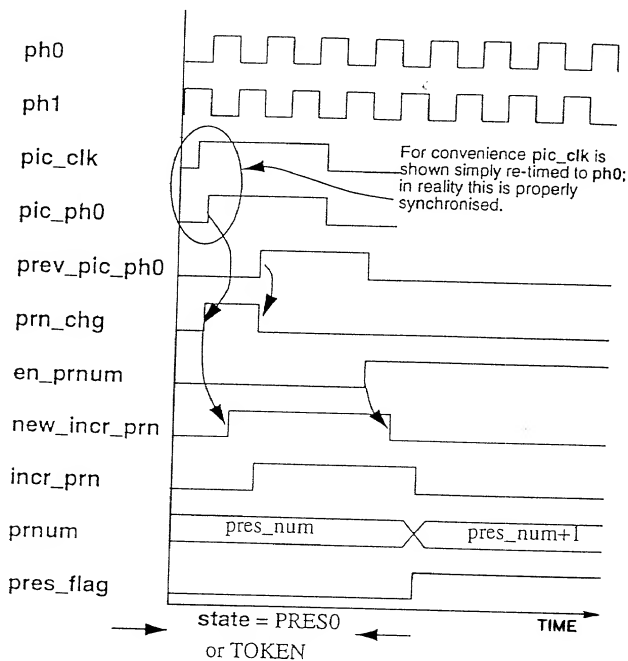


FIG. 156

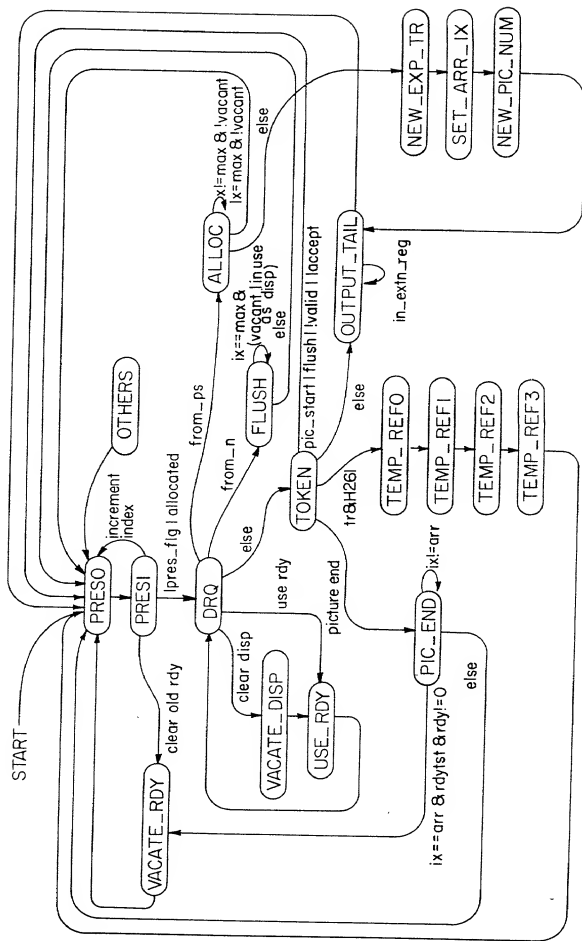


FIG. 157

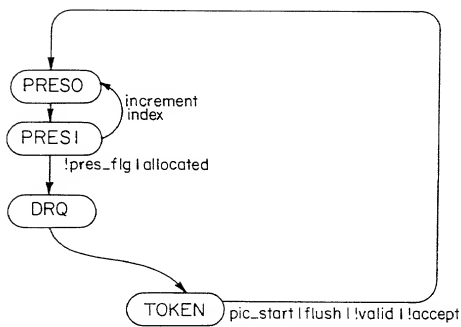
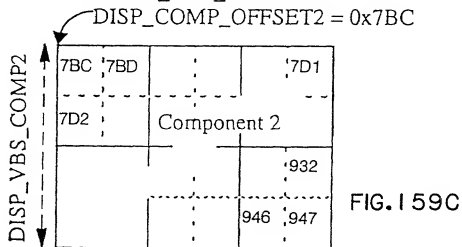
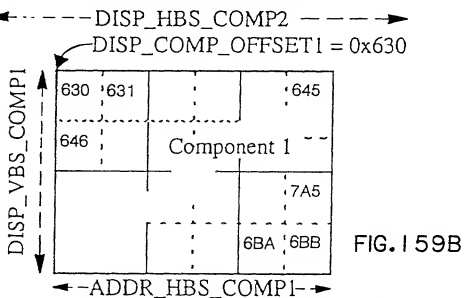
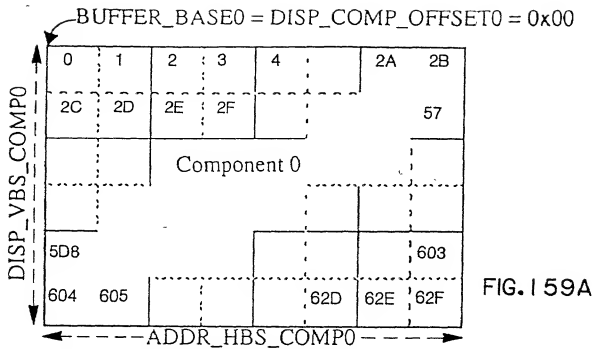


FIG. 158



BUFFER OFFSET 0x00

COMPONENT OFFSET 0x000 +

| | | | | | | | | | | | |
|----|----|----|----|----|----|----|----|----|----|----|----|
| 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 | 0A | 0B |
| 0C | 0D | 0E | 0F | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
| 18 | 19 | 1A | 1B | 1C | 1D | 1E | 1F | 20 | 21 | 22 | 23 |
| 24 | 25 | 26 | 27 | 28 | 29 | 2A | 2B | 2C | 2D | 2E | 2F |
| 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 3A | 3B |
| 3C | 3D | 3E | 3F | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| 48 | 49 | 4A | 4B | 4C | 4D | 4E | 4F | 50 | 51 | 52 | 53 |
| 54 | 55 | 56 | 57 | 58 | 59 | 5A | 5B | 5C | 5D | 5E | 5F |
| 60 | 61 | 62 | 63 | 64 | 65 | 66 | 67 | 68 | 69 | 6A | 6B |
| 6C | 6D | 6E | 6F | 70 | 71 | 72 | 73 | 74 | 75 | 76 | 77 |
| 78 | 79 | 7A | 7B | 7C | 7D | 7E | 7F | 80 | 81 | 82 | 83 |
| 84 | 85 | 86 | 87 | 88 | 89 | 8A | 8B | 8C | 8D | 8E | 8F |

FIG.161A

COMPONENT1 OFFSET 0x100 +

| | | | | | |
|----|----|----|----|----|----|
| 00 | 01 | 02 | 03 | 04 | 05 |
| 06 | 07 | 08 | 09 | 0A | 0B |
| 0C | 0D | 0E | 0F | 10 | 11 |
| 12 | 13 | 14 | 15 | 16 | 17 |
| 18 | 19 | 1A | 1B | 1C | 1D |
| 1E | 1F | 20 | 21 | 22 | 23 |

FIG.161B

COMPONENT1 OFFSET 0x200 +

| | | | | | |
|----|----|----|----|----|----|
| 00 | 01 | 02 | 03 | 04 | 05 |
| 06 | 07 | 08 | 09 | 0A | 0B |
| 0C | 0D | 0E | 0F | 10 | 11 |
| 12 | 13 | 14 | 15 | 16 | 17 |
| 18 | 19 | 1A | 1B | 1C | 1D |
| 1E | 1F | 20 | 21 | 22 | 23 |

FIG.161C

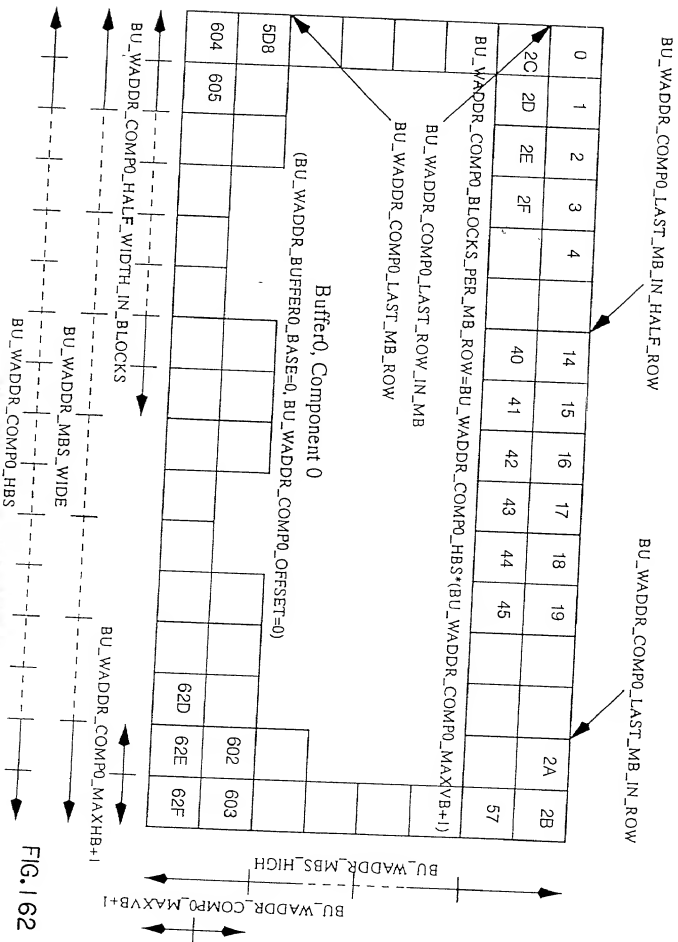


FIG. 162

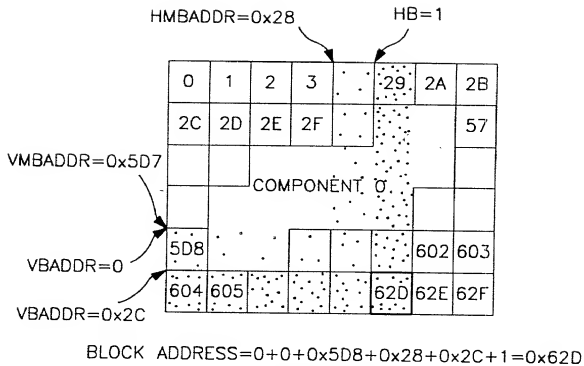


FIG. 1 63A

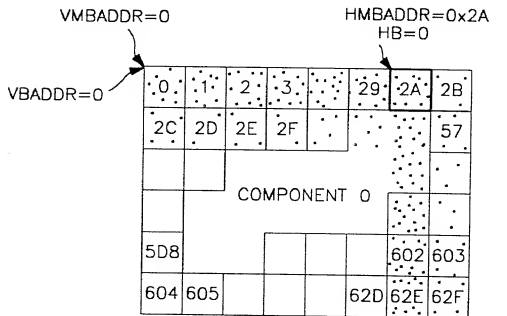


FIG. 1 63B

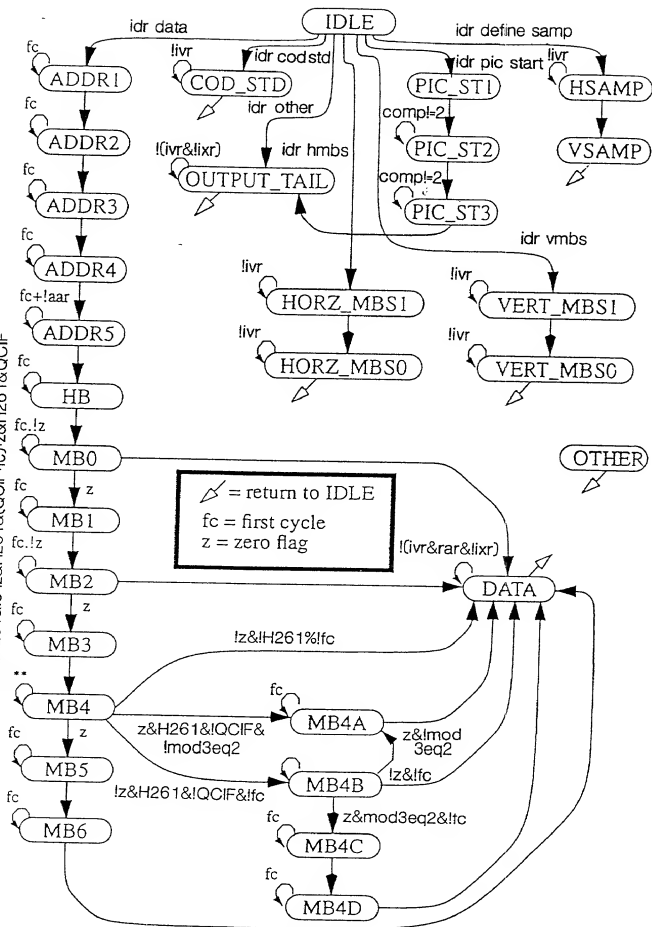


FIG. 164

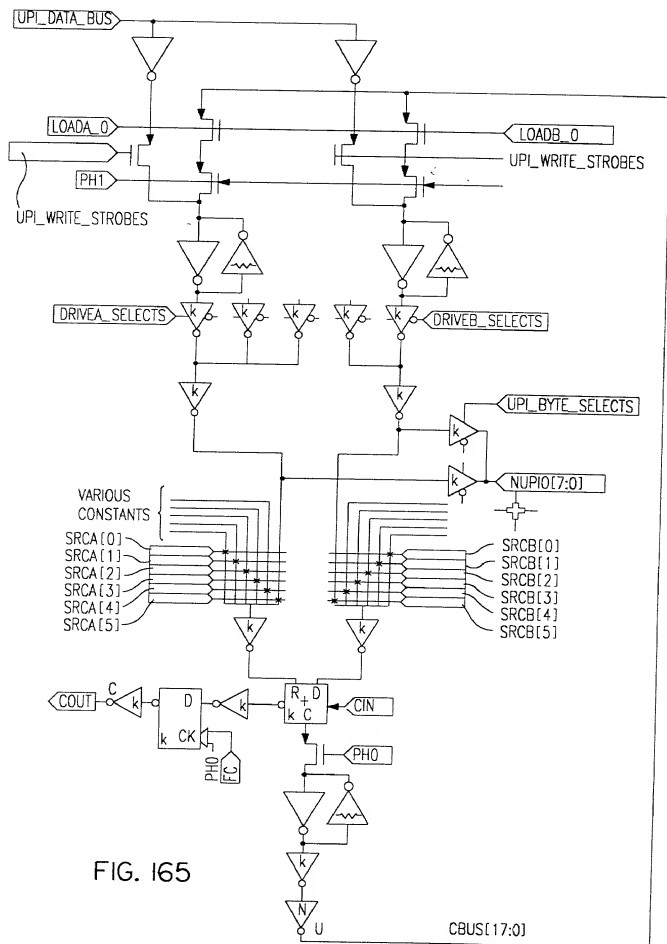
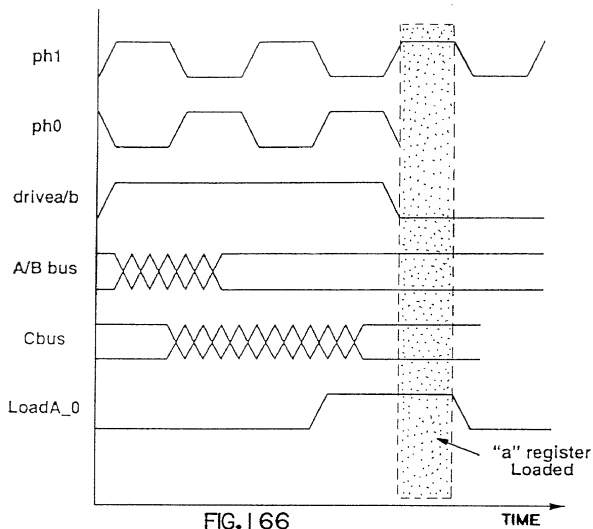


FIG. 165



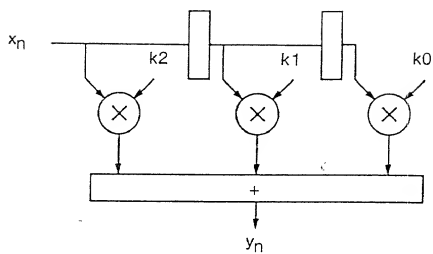


FIG. 167

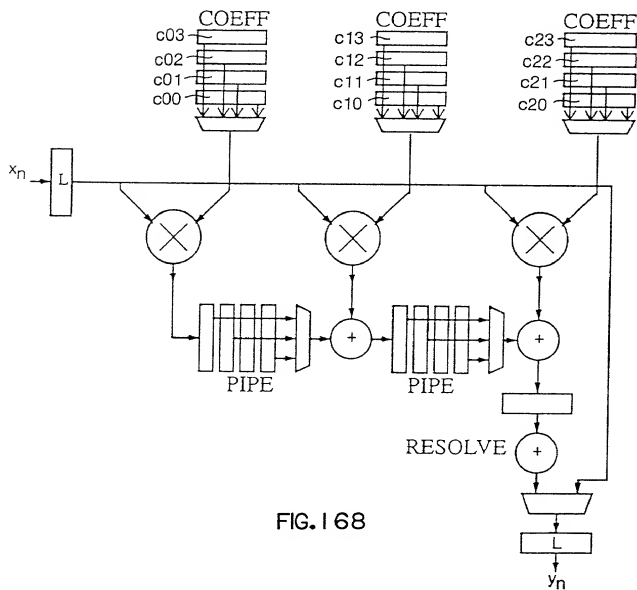


FIG. 168

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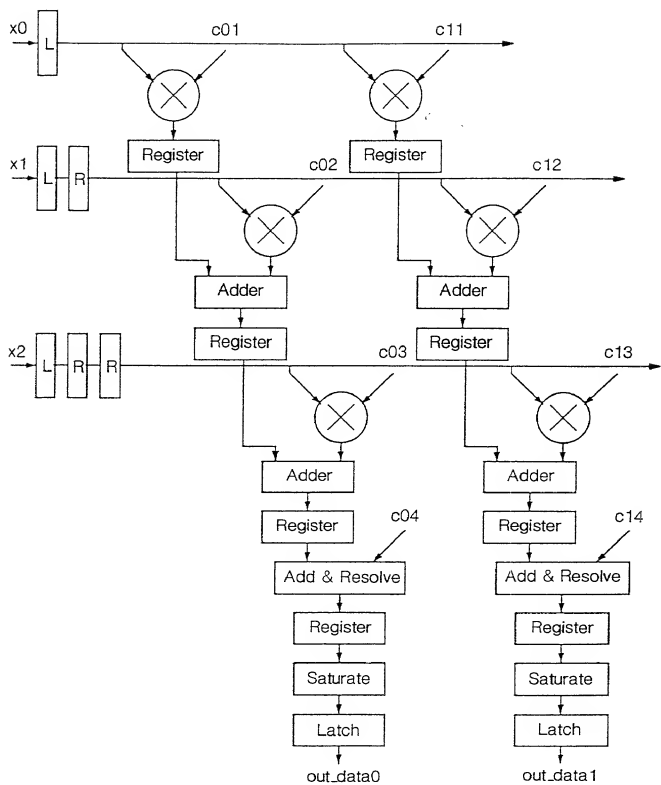


FIG. 1 69